

FPGA BASED CONTROLLER CARD FOR DATA ACQUISITION SYSTEM

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Abstract— Data acquisition is the process of measuring real world physical conditions and converting it into digital numeric values. A typical data acquisition system consists of (i) Sensors that convert physical parameters to electrical signals, (ii) Signal conditioning circuitry, (iii) Analog to Digital Convertors [1]. For Sound Navigation and Ranging (SONAR) front end application specific data acquisition systems, a controller card is required which controls the transmission of data that is received. In this paper, the focus is for an efficient controller card development by using the Virtex – 5 FPGA (Field Programmable Gate Array). FPGAs have soft IPs (Intellectual Property) and hard IPs that can be used on demand. Here the controller card is based on a soft processor microblaze. The use of soft processor reduces the complexity of developing the controller card with an FPGA and an external processor as a controller since the soft processor exists on the same FPGA. This creates a highly robust and reliable system.

Keywords— FPGA; Microblaze; Intellectual Property (IP); SONAR; Human Machine Interface (HMI); Xilinx Platform Studio (XPS); Software Development Kit (SDK)

INTRODUCTION

The data acquisition system receives the data from sensors and is converted to digital form by the Analog to Digital (ADC) cards. The data in digital form is fed from ADC cards to the controller card. Controller card has two regions, an embedded processor and a transceiver hardware section. Embedded processor communicates with the HMI through which necessary control data is taken. Depending on the instructions given by the HMI to the embedded processor, data received from ADC cards are routed to required destination. Virtex5LXT FPGAs have microblaze soft processors and peripherals like UART (Universal Asynchronous Receiver/Transmitter), Ethernet, DDR2 SDRAM (Double Data Rate Synchronous Dynamic Random-Access Memory), Flash etc. as soft IPs. Microblaze is a 32 bit Reduced Instruction Set Computing (RISC) processor [5]. The peripherals can be instantiated based on the requirement to create an embedded system inside the FPGA. Here, an embedded soft processor based controller is developed for SONAR front end application.

METHODOLOGY

ML505 evaluation board based on Virtex 5 FPGA of Xilinx is used for the system development. Block diagram of controller card is shown in Figure -1. The transceiver takes the configuration data from the block RAM (Random Access Memory) which is written by the soft processor. This paper focuses on development of microblaze soft processor based controller.

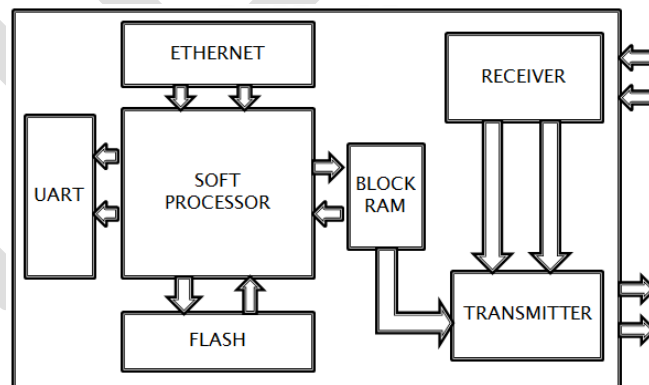


Figure – 1: Block diagram of controller card

Hardware Design

The embedded controller hardware is developed in XPS by instantiating the microblaze soft processor with peripherals UART, Ethernet, Flash and a custom memory peripheral generated from core generator. This custom memory peripheral is the bridge between the transceiver and the embedded processor.

The microblaze processor is instantiated with clock 125MHz and local memory of 64KB. UART and Ethernet forms the Human Machine Interface. The configuration details of the system and any debugging information are shown on the PC through the Tera Term/ Hyper Terminal using the UART 16550 through the RS232 cable. The Ethernet configured was a hard Ethernet MAC which could support speed up to 1Gps and is configured in Gigabit Media Independent Interface (GMII) mode with required jumper settings [6]. The custom Block RAM was made with 32 bit width and 1024 bit depth from the IP Core and the custom Block RAM (BRAM) was added by using the IP – IC (Intellectual Property – Inter-Connect) interface. It was done so because the BRAM must be common to hardware transceiver and the embedded controller. The control data was written to BRAM through the Ethernet and based upon the control data the transceiver would work.

The microblaze soft processor accesses its peripherals using Processor Local Bus [8]. Hence a Processor Local Bus top module is written over the custom memory in order to import the memory peripheral to microblaze processor using the IP – IC interface technology. Intel JS28F256P30T95 BPI flash is used to take back up of last configuration data in BRAM [4].

Software Design

The hardware design is exported on to the SDK to start with the embedded programming. Upon this hardware, a Board Support Package is made. The BSP was made such that the microblaze processor was loaded with Xilkernel OS [3]. Xilkernel is a small, robust, and modular kernel. It is highly integrated with the Platform Studio framework and is a free software library that is available with the Xilinx Embedded Development Kit (EDK) [9]. It allows a very high degree of customization, letting users tailor the kernel to an optimal level both in terms of size and functionality. To this BSP lwIP and xilflash are added for the Ethernet and flash support [11]. Since the design is based on Xilkernel OS, the lwIP is configured in socket mode [7]. The main advantage of Xilkernel OS is multithreading functionality.

Software design can be divided into three sections. The first section includes the startup procedure to initialize the UART along with a programming to assign specific IP address and MAC address to the board. The second section does the reception of packet and extracting the data to write into the BRAM. The third section does the initialization of flash and unlocking the specific memory areas to write the same data from BRAM to flash.

IMPLEMENTATION

The hardware implemented is shown in Figure – 2. The microblaze processor is instantiated with peripherals UART, Ethernet, DDR2, Flash and custom memory core. It could be seen that the microblaze processor communicates with the peripherals using the Processor Local Bus (PLB) and Local Memory Bus (LMB) is used to access the local memory Tools used is Xilinx 13.3 ISE/EDK, Lab VIEW, Wire shark and Tera Term.

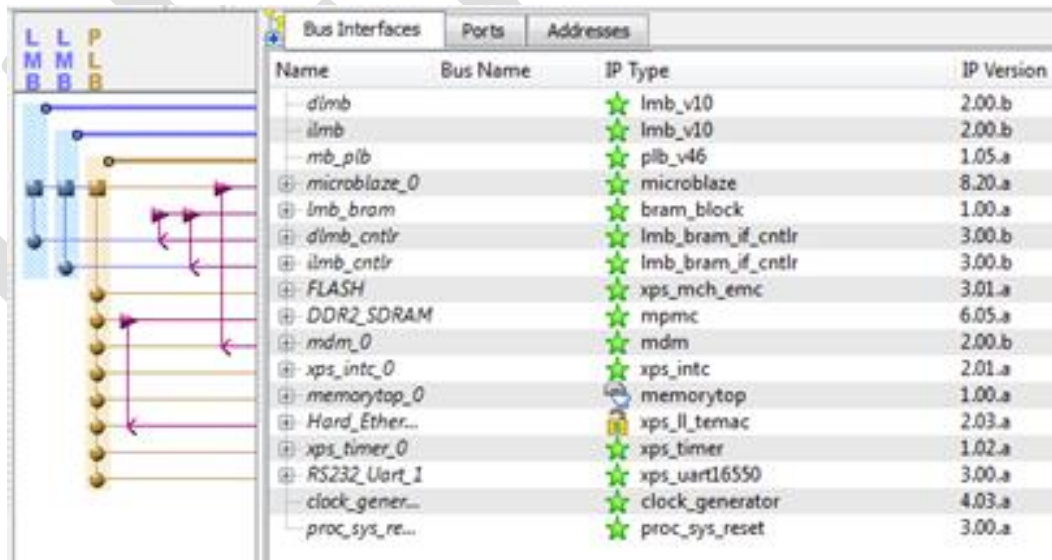


Figure – 2: XPS view of the hardware

Figure – 3 shows the addresses mapped to each of the microblaze peripherals. The memory added is assigned an address space of 1K and the starting address is 0x89840000. The Flash address starts at 0x8C000000 and has a size of 32M.

Instance	Base Name	Base Address	High Address	Size	Bus Interface(s)	Bus Name
microblaze_0's Address Map						
dlimb_cntlr	C_BASEADDR	0x00000000	0x0000FFFF	64K	SLMB	dlimb
ilmb_cntlr	C_BASEADDR	0x00000000	0x0000FFFF	64K	SLMB	ilmb
xps_intc_0	C_BASEADDR	0x81800000	0x8180FFFF	64K	SPLB	mb_plib
xps_timer_0	C_BASEADDR	0x83C00000	0x83C0FFFF	64K	SPLB	mb_plib
RS232_Uart_1	C_BASEADDR	0x83E00000	0x83E0FFFF	64K	SPLB	mb_plib
mdm_0	C_BASEADDR	0x84400000	0x8440FFFF	64K	SPLB	mb_plib
DDR2_SDRAM	C_SDMA_CTRL_BASEADDR	0x84600000	0x8460FFFF	64K	SDMA_CTRL1	mb_plib
Hard_Ethernet_MAC	C_BASEADDR	0x87000000	0x8707FFFF	512K	SPLB	mb_plib
memorytop_0	C_BASEADDR	0x89840000	0x898403FF	1K	SPLB	mb_plib
FLASH	C_MEM0_BASEADDR	0x8C000000	0x8DFFFFFFFF	32M	SPLB	mb_plib
DDR2_SDRAM	C_MPMC_BASEADDR	0x90000000	0x9FFFFFFF	256M	SPLB0:SDMA_LLI	mb_plib:Hard_Et...

Figure – 3: Address mapped to each peripherals

This implemented hardware is ported to SDK tool for writing the embedded code. Figure – 4 shows the SDK view of the system developed.

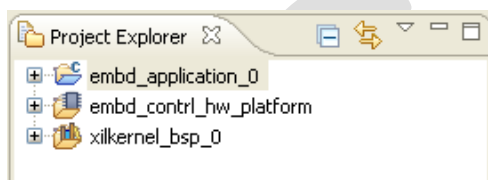


Figure – 4: SDK view of the system

RESULTS

An embedded soft processor controller was developed on ML505 board for SONAR front end application and the coding was done in embedded C [12]. The protocol supports provided include Internet Protocol (IP), Internet Control Message Protocol (ICMP), User Datagram Protocol (UDP), Transmission Control Protocol (TCP), and Internet Group Message Protocol (IGMP) [10]. The system was configured with IP address 192.168.1.100 [2]. The ping command was used to verify the ICMP protocol. TCP protocol was verified by checking the correctness of data by sending it back to PC. A UDP packet was send from lab view and that data was extracted and written on to the custom memory peripheral.

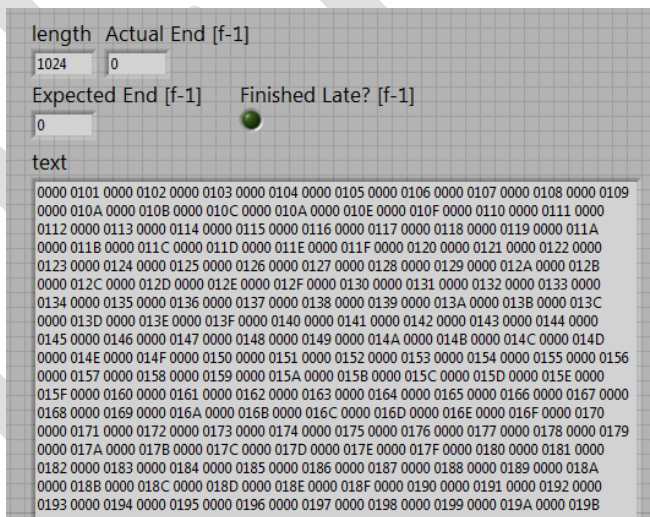


Figure – 5: Lab view providing inputs

The UART output in Tera Term shows the board configuration details initially. Tera Term screen shot is shown in Figure – 6. Once the UDP packet is received by the system, the received number of bytes and the data written to each memory location is displayed which validates the input data. After the completion of data writing to the custom memory, back up of same data is taken by writing the same to flash memory.

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CONFIGURATION DETAILS
Board IP: 192.168.1.100
Netmask : 255.255.255.0
Gateway : 192.168.1.1

auto-negotiated link speed: 1000
No. of bytes = 400

Value in Memory_Address 89840000 = 1
Value in Memory_Address 89840004 = 2
Value in Memory_Address 89840008 = 3
Value in Memory_Address 8984000C = 4
Value in Memory_Address 89840010 = 5
Value in Memory_Address 89840014 = 6
Value in Memory_Address 89840018 = 7
Value in Memory_Address 8984001C = 8
Value in Memory_Address 89840020 = 9
Value in Memory_Address 89840024 = A
Value in Memory_Address 89840028 = B
Value in Memory_Address 8984002C = C
Value in Memory_Address 89840030 = A
Value in Memory_Address 89840034 = E
Value in Memory_Address 89840038 = F
Value in Memory_Address 8984003C = 10
Value in Memory_Address 89840040 = 11
Value in Memory_Address 89840044 = 12
Value in Memory_Address 89840048 = 13
Value in Memory_Address 8984004C = 14
Value in Memory_Address 89840050 = 15
Value in Memory_Address 89840054 = 16
Value in Memory_Address 89840058 = 17
Value in Memory_Address 8984005C = 18
Value in Memory_Address 89840060 = 19
Value in Memory_Address 89840064 = 1A
Value in Memory_Address 89840068 = 1B
Value in Memory_Address 8984006C = 1C
Value in Memory_Address 89840070 = 1D
Value in Memory_Address 89840074 = 1E
Value in Memory_Address 89840078 = 1F
Value in Memory_Address 8984007C = 20
Value in Memory_Address 89840080 = 21
Value in Memory_Address 89840084 = 22
Value in Memory_Address 89840088 = 23
Value in Memory_Address 8984008C = 24
Value in Memory_Address 89840090 = 25
Value in Memory_Address 89840094 = 26
Value in Memory_Address 89840098 = 27
Value in Memory_Address 8984009C = 28
Value in Memory_Address 898400A0 = 29
Value in Memory_Address 898400A4 = 2A
Value in Memory_Address 898400A8 = 2B

Value in Memory_Address 8984037C = E0
Value in Memory_Address 89840380 = E1
Value in Memory_Address 89840384 = E2
Value in Memory_Address 89840388 = E3
Value in Memory_Address 8984038C = E4
Value in Memory_Address 89840390 = E5
Value in Memory_Address 89840394 = E6
Value in Memory_Address 89840398 = E7
Value in Memory_Address 8984039C = E8
Value in Memory_Address 898403A0 = E9
Value in Memory_Address 898403A4 = EA
Value in Memory_Address 898403A8 = EB
Value in Memory_Address 898403AC = EC
Value in Memory_Address 898403B0 = ED
Value in Memory_Address 898403B4 = EE
Value in Memory_Address 898403B8 = EF
Value in Memory_Address 898403BC = F0
Value in Memory_Address 898403C0 = F1
Value in Memory_Address 898403C4 = F2
Value in Memory_Address 898403C8 = F3
Value in Memory_Address 898403CC = F4
Value in Memory_Address 898403D0 = F5
Value in Memory_Address 898403D4 = F6
Value in Memory_Address 898403D8 = F7
Value in Memory_Address 898403DC = F8
Value in Memory_Address 898403E0 = F9
Value in Memory_Address 898403E4 = FA
Value in Memory_Address 898403E8 = FB
Value in Memory_Address 898403EC = FC
Value in Memory_Address 898403F0 = FD
Value in Memory_Address 898403F4 = FE
Value in Memory_Address 898403F8 = FF
Value in Memory_Address 898403FC = 100

success XFlash_Initialize
success XFlash_Reset
success XFlash_Unlock
success XFlash_Erase
success XFlash_Write
Value in Memory_Address 8C010000 = 1
Value in Memory_Address 8C010004 = 2
Value in Memory_Address 8C010008 = 3
Value in Memory_Address 8C01000C = 4
Value in Memory_Address 8C010010 = 5
Value in Memory_Address 8C010014 = 6
Value in Memory_Address 8C010018 = 7
Value in Memory_Address 8C01001C = 8
Value in Memory_Address 8C010020 = 9
Value in Memory_Address 8C010024 = A
Value in Memory_Address 8C010028 = B
Value in Memory_Address 8C01002C = C
Value in Memory_Address 8C010030 = A
Value in Memory_Address 8C010034 = E
Value in Memory_Address 8C010038 = F

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Figure – 6: Display in Tera Term

Wire shark was used as a monitoring tool which showed the data sent and the protocol followed by the data. It is shown in Figure – 7.

No.	Time	Source	Destination	Protocol	Info
24	2.345297	90.b1.1c.9d.2a.f8	01:00:00:00:00:00	ARP	Who has 192.168.1.100? sent 192.168.1.1
25	2.548610	xilinx_00:01:02	90.b1.1c.9d.2a:f8	ARP	192.168.1.100 is at 00:0a:35:00:01:02
26	2.548610	192.168.1.1	192.168.1.100	UDP	Source port: 52002 Destination port: 52002
27	2.550702	192.168.1.1	192.168.1.255	NBNS	Name query NB ISATAP<0>
28	3.024552	fe80::b1e8:d5c:f777:3	ff02::1:2	DHCPv6	Solicit
29	3.300499	192.168.1.1	192.168.1.255	NBNS	Name query NB ISATAP<0>
30	3.413685	192.168.1.1	239.255.255.250	SSDP	M-SEARCH * HTTP/1.1
31	4.050730	192.168.1.1	192.168.1.255	NBNS	Name query NB ISATAP<0>
32	4.332460	fe80::b1e8:d5c:f777:3	ff02::1:2	ICMPv6	Router solicitation
33	4.465611	192.168.1.1	239.255.255.250	SSDP	M-SEARCH * HTTP/1.1
34	4.490592	192.168.1.1	239.255.255.250	SSDP	M-SEARCH * HTTP/1.1
35	5.827842	fe80::b1e8:d5c:f777:3	ff02::1:3	UDP	Source port: 54118 Destination port: 11mnr
36	5.828175	192.168.1.1	224.0.0.252	UDP	Source port: 58642 Destination port: 11mnr
37	5.927533	fe80::b1e8:d5c:f777:3	ff02::1:3	UDP	Source port: 54118 Destination port: 11mnr
38	5.927649	192.168.1.1	224.0.0.252	UDP	Source port: 58642 Destination port: 11mnr

Frame 26 (1066 bytes on wire, 1066 bytes captured)					
Ethernet II, Src: 90:b1:1c:9d:2a:f8 (90:b1:1c:9d:2a:f8), Dst: xilinx_00:01:02 (00:0a:35:00:01:02)					
Internet Protocol, Src: 192.168.1.1 (192.168.1.1), Dst: 192.168.1.100 (192.168.1.100)					
User Datagram Protocol, Src Port: 52002 (52002), Dst Port: 52002 (52002)					
Data (1024 bytes)					

0020	01 64 cb 22 cb 22 04 08 5d 65 00 00 00 01 00 00	.d."..]e.....
0030	00 02 00 00 00 03 00 00 00 04 00 00 00 05 00 00
0040	00 06 00 00 00 07 00 00 00 08 00 00 00 09 00 00
0050	00 0a 00 00 00 0b 00 00 00 0c 00 00 00 0d 00 00
0060	00 0e 00 00 00 0f 00 00 00 10 00 00 00 11 00 00
0070	00 12 00 00 00 13 00 00 00 14 00 00 00 15 00 00
0080	00 16 00 00 00 17 00 00 00 18 00 00 00 19 00 00
0090	00 1a 00 00 00 1b 00 00 00 1c 00 00 00 1d 00 00
00a0	00 1e 00 00 00 1f 00 00 00 20 00 00 00 21 00 00
00b0	00 22 00 00 00 23 00 00 00 24 00 00 00 25 00 00
00c0	00 26 00 00 00 27 00 00 00 28 00 00 00 29 00 00
00d0	00 2a 00 00 00 2b 00 00 00 2c 00 00 00 2d 00 00
00e0	00 2e 00 00 00 2f 00 00 00 30 00 00 00 31 00 00
00f0	00 32 00 00 00 33 00 00 00 34 00 00 00 35 00 00
0100	00 36 00 00 00 37 00 00 00 38 00 00 00 39 00 00
0110	00 3a 00 00 00 3b 00 00 00 3c 00 00 00 3d 00 00
0120	00 3e 00 00 00 3f 00 00 00 40 00 00 00 41 00 00
0130	00 42 00 00 00 43 00 00 00 44 00 00 00 45 00 00

Figure – 7: Wire shark view

ACKNOWLEDGEMENT

The authors wish to thank Director, NPOL for permitting to carry out this project. Authors also wish to thank Mr. Suresh M., Scientist

G, NPOL, Mrs. Jayamma T. M., Scientist F, NPOL, Ralph D Kappithan and Scientist D, NPOL for their valuable guidance, help and insightful comments.

CONCLUSION

Soft processor based FPGA controller card is a promising reliable and robust system for SONAR front end applications. The hardware was built by instantiating microblaze soft processor with UART, Ethernet, Flash and custom memory as peripherals. On this hardware an embedded system was developed which receives data in UDP packet and extract the data to write to the custom memory and a backup of data was taken in flash simultaneously. The system was implemented on Xilinx ML505 board and the required functionalities were verified. Here a highly efficient system is suggested which reduces the handshake unreliability between the hardware and the processor that becomes a big bottle neck while designing controller cards.

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