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DESIGN AND IMPLEMENTATION OF HIGH SPEED LFSR USING MCML LOGIC

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Abstract— LFSR, Linear Feedback Shift Register is one of the key element in the high speed VLSI testing to generate pseudo random bits. In this paper, High speed 5GHz LFSR is implemented using MOS current mode logic. Cadence virtuoso 0.18um technology is used to implement the proposed logic. Simulated results of the proposed logics are presented.
Keywords— LFSR, MCML, Pseudo random bits, Virtuoso

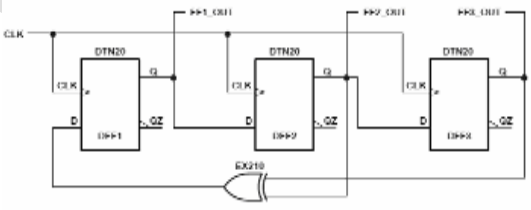
INTRODUCTION

In large scale integration, millions of transistors can be placed on a single chip for implementation of complex circuitry. As a result of placing so many transistors in such a small space, major problems of power consumption had come into the picture. Research has been conducted to solve these problems. Solutions have been proposed to decrease the power supply voltage, switching frequency and capacitance of transistor [1]. Linear Feedback Shift Register LFSR is a Pseudo Random Sequence Generator used in a variety of applications such as Built-in-self test (BIST) [2], cryptography, error correction code and in field of communication. In cryptography it is used to generate public and private keys. Today LFSR's are present in nearly every coding scheme as they produce sequences with good statistical properties, and they can be easily analyzed. Moreover they have a low-cost realization in hardware. Counters such as Binary, Gray suffer problem of power consumption, glitches, speed, and delay because they are implemented with techniques which have above drawbacks. They produce not only glitches, which increase power consumption and design complexity. The propagation delay of the existing techniques is more which reduces speed and performance of system. In this paper 5GHz LFSR is designed using MOS Current Mode Logic (MCML). The speed of the testing device in BIST can be increased by using high speed LFSR.

LFSR

A **linear feedback shift register** (LFSR) is a shift register whose input bit is a linear function of its previous state. The initial value of the LFSR is called the seed, and because the operation of the register is deterministic, the stream of values produced by the register is completely determined by its current (or previous) state. Likewise, because the register has a finite number of possible states, it must eventually enter a repeating cycle. However, an LFSR with a well-chosen feedback function can produce a sequence of bits which appears random and which has a very long cycle. Applications of LFSRs include generating pseudo-random numbers and fast digital counters. LFSR is basically, a shift register configuration that propagates the stored patterns from left to right. The modification that provides the Pseudo Random Sequence Generator which generates the output due to the XOR feedback of the selected flip-flop outputs, named taps. When the taps are chosen properly, the LFSR will traverse through all possible states except for the all 0s state and will produce a maximum length pseudo random bit sequence (PRBS) named M-sequence. In order for the desired operation, the LFSR should be first initialized to a well-known stage, as seed. For an n stage LFSR, there are 2n-1 states, and the M sequence is 2n-1 bits long. Hence, the M-sequence is periodic, and after the 2n-1 distinct values, it repeats itself in the next samples. Block diagram of 3-bit LFSR is depicted in fig 1.

Figure:1



Linear Feedback Shift Registers

List of bits that effects the next state are called tap sequence that is the outputs that influences the input are called taps. The tap sequence of an LFSR can be represented as a polynomial mod 2 that is coefficients of polynomial is either 0 or 1 this is called feed back polynomial or characteristics polynomial. If (and only if) this polynomial is a primitive, then the LFSR is maximal. The LFSR

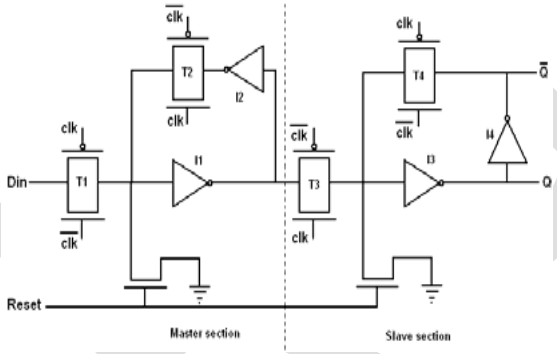
will only be maximal if the number of taps are even. The tap values in a maximal LFSR will be relatively prime. There can be more than one maximal tap sequence for a given LFSR length. Its output for the various condition of input is expressed in Table1.

Table 1. Truth table for LFSR

Clock pulse	FF1	FF2	FF3
1	1	1	1
2	1	1	0
3	1	0	0
4	0	0	1
5	0	1	0
6	1	0	1
7	0	1	1

In literature each D-FF of LFSR is implemented by using either transmission gates or pass transistor. Circuit diagram of D-FF using transmission gates are depicted in fig.2.

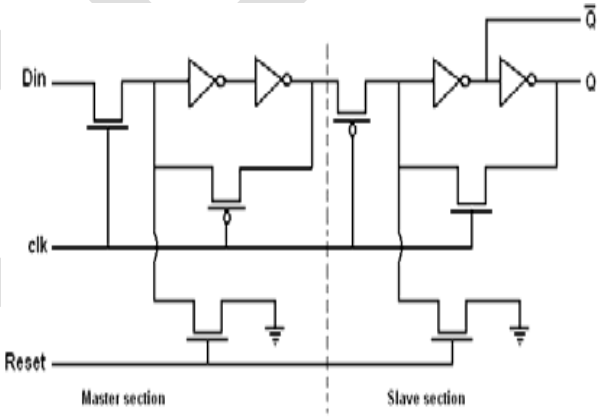
Figure:2



LFSR using TG

Totally it requires 18 transistor to implement the above design. One more is implementation of D-FF using pass transistor logic is implemented in fig.3.

Figure:3



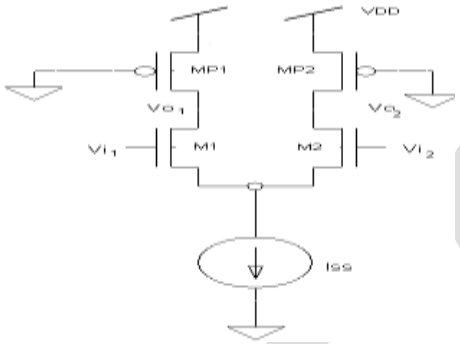
LFSR using pass transistor

In this design DFF using pass transistor logic requires 14 transistors. For both transmission gate and pass transistor based techniques the maximum frequency of operation is 1.7GHz.

MCML

MCML circuits are based on current steering logic where in current is ideally steered by a one of the branches depending on the inputs at the NMOS transistor. Advantages of MOS current mode logic have high noise immunity due to its differential nature. It achieves high speed by consuming less power and high supply noise rejection.

Figure:4



MCML inverter

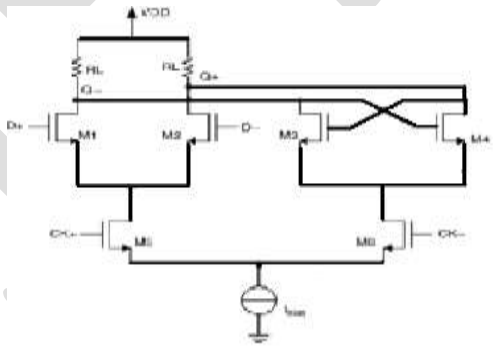
PMOS load is forced to work in linear region of operation resistance of PMOS along with current flowing through it determines voltage swing at the output. The NMOS input transistors are employed to perform the required logic operation. Current source is used to provide a constant current through the circuit so as to reduce the fluctuations from the power lines and maintain constant power consumption irrespective of frequency of operation. For better and faster operation NMOS transistor of MCML circuit forced to operate in saturation region.

DIFFERENT MCML TOPOLOGIES

MCML D Latch

MCML D latch is depicted in fig.5. It consist of two parts one is MCML inverter and second is latch circuit. During positive half cycle data from transistor M1 and M2 are inverted and during negative cycle inverted data is latched.

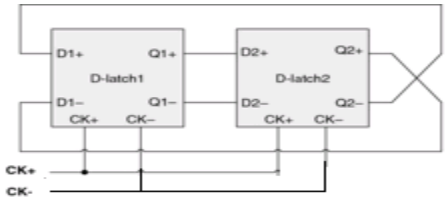
Figure:5



MCML D latch

Circuit diagram of master slave D flip flop is depicted in fig .6

Figure:6

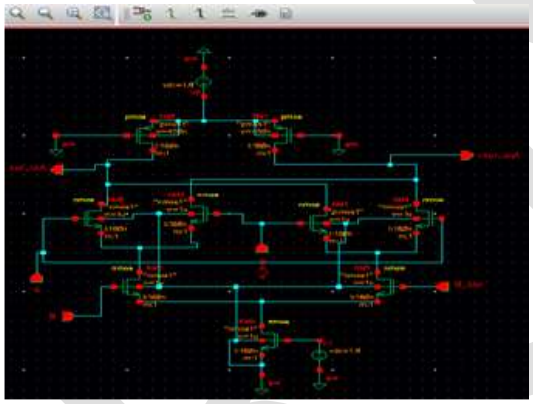


MS D flip flop

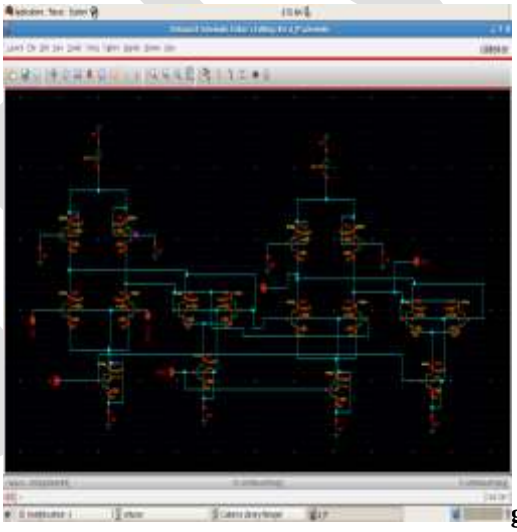
EXPERIMENTAL RESULTS

Circuit diagram of MCML XOR gate is depicted in fig.7

Figure:7



MCML XOR gate

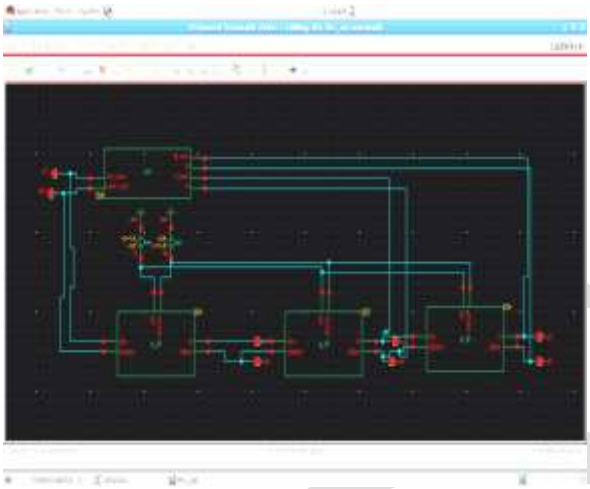


gure:8

MS D flip flop

The circuit diagram of master slave D flipflop is depicted in fig.8

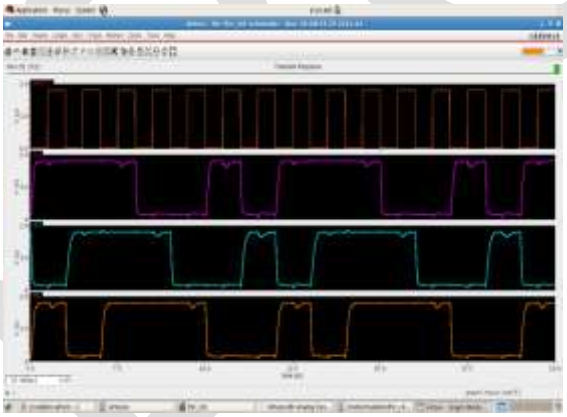
Figure:9



LFSR using MCML XOR and MCML MS D- FF

The circuit diagram of LFSR with a polynomial X^3+X^2+1using MCML XOR gate and MCML master slave D FF is depicted in fig.9.The pseudo random sequences are generated using MCML LFSR. The proposed LFSR works until 5 GHz with out any distortion. Waveforms of the proposed LFSR for 5 GHz is depicted in fig.10

Figure:10



Waveforms of the proposed LFSR for 5 GHZ

CONCLUSION

In Table II indicates different LFSR for different parameters such as number of transistors, power dissipation, maximum frequency of operation and area required to construct the LFSR. Table II indicates that proposed LFSR is optimized in all the parameters.

LFSR	Number of transistor	Power (uW)	Maximum frequency (GHz)	Area mm^2
Transmission Gate	86	99.6	1.7	270
Pass Transistor	68	28.188	1.4	321
Proposed	**56**	**21.12**	**5**	

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