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Low leakage Architecture of Static Random Access Memory using LECTOR Technique

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Abstract—The integrated circuits that have memories, a major share of total circuit power is required by the memory architecture of the circuit. With the day-to-day changing circuit designs, the need to store increasing amount of processing data has resulted in the growing memory size in an integrated circuit. Most of the memory data remains un-altered during the memory data handling operation. The stored data is thus affected by the sub-threshold leakage power / current that leads to the degradation of data signal quality. The data integrity is maintained using a feedback path / architecture in SRAM memory architecture. Still, the amount of power loss due to leakage contributes a major part of the total power loss of the integrated circuit. This loss increases with the decrease in the physical feature size of the component / transistors. A low power system offers the benefits like device portability, long battery life, good performance criteria, etc. Today's increasing data handling require more random access memory to process the dynamic data and hence more power. Various SRAM architectures and its Design techniques are proposed in previous work. SRAM low power design using Sleepy Stack Transistor for is proposed by S.Lakshmi Narayan et al [1]. Dynamic Threshold and Stand-by Voltage leakage reduction technique is presented by Yashwant Singh and D. Boolchandani in [2].Power reduction using Power Gating is shown by AdreaCalimera et al [3]. Static Power Reduction Techniques for Asynchronous circuits is given by Carlos Ortega, Jonathan Tse and RajitManohar in [4]. These are some suggested techniques that can offer a solution towards low power in the design of SRAM architecture.In the present work, we have used leakage control transistor technique called LECTOR to modify the design of SRAM architecture to reduce the leakage current and hence the leakage power. The absence of requirement of control circuit for the operation of leakage control transistor in this technique is the major advantage of LECTOR technique over the other available leakage current reduction techniques. The proposed design is simulated on 90nm CMOS fabrication technology using Microwind Tool.

Keywords— Address Decoder, CMOS, Dynamic Power, Leakage Control Transistor, Load Line Capacitance, Memory Array, SRAM, Subthreshold Leakage Current, Threshold Voltage, Microwind.

INTRODUCTION

The basis requirement of any Integrated Circuit is high speed and low power processing of the data signals to perform the desired execution. The minimization of feature size plays an important role in increasing the performance of integrated circuits. But the feature minimization inversely affects the percentage of leakage current when compared to the total current requirement of the circuit. The main causes of the dissipation of power are: 1) short-circuit current, 2) load capacitance charging and discharging current, and 3) transistor leakage current in the sub-threshold operating condition. The data value transition activity during memory data processing is the main cause of short circuit power dissipation. There are various proposed techniques to reduce the short circuit current dissipation but at the cost of extra control and monitoring circuit. This additional circuit further contributes in the dissipation of power. The improving semiconductor processing techniques have made it possible to reduce the size of memories leading to a higher density of memory elements per square unit of area. This has also contributed in decreasing the power dissipation by reducing the load charging and discharging current due to smaller size of the parasitic capacitance of the load capacitors. The leakage current is more effective in deep sub-micron technologies. A number of leakage reduction techniques for CMOS based transistor level design and techniques have been proposed in previous works like leakage lector techniquefor CMOS circuits by H. Narender and R. Nagarajan[5],SonamRathore[6], P. Verma and R. A. Mishra[7] andB. Dilip et al[8].The previously proposed design techniques are Transistor stack based low leakage approach by M. C. Johnson et al[9],sleeper keeper technique for leakage reduction by S. H. Kim and V. J. Mooney[10], Resource allocation and binding approach by C. Gopalakrishnan and S. Katkoori[11], scaling of stack for leakage reduction byS. Narendra et al [12], gate level design modification for low power CMOS by J. P. Halter and F. Najm [13], etc. Multiple Threshold Transistor Design Technique is proposed by V. Sundarajan and K. K. Parhi [14], Q. Wang and S. Vrudhula [15]. Gated-Clock based low power design is referenced as proposed by J. Shinde and S. S. Salankar [16],M. D. Powellet al[17]. Various proposed techniques provide benefits with respect to specific design application.

LECTOR TECHNIQUE IN CMOS CIRCUIT DESIGN

Lector approach to reduce leakage current is based on the effective stacking of transistors between the supply voltages to the ground voltage. In Lector approach two leakage control transistors are introduced between the conventional pull-up and pull-down logic circuits of a functional block. For example, the conventional CMOS NAND Gate circuit is shown in Fig-1 and the Lector based CMOS NAND Gate circuit is shown in Fig-2. The wiring configuration in the Lector approach ensures that one of the two leakage control transistors is always near its cut-off region of operation irrespective of the input voltage. The Lector follows the concept that, "a state with more than one transistor OFF in a path between supply and ground voltage is less leaky than a state with only one transistor OFF between any supply and ground path". Thus the lector approach leads to a current limited resistive path between the supply voltages to reduce the leakage power dissipation through the lector circuit.

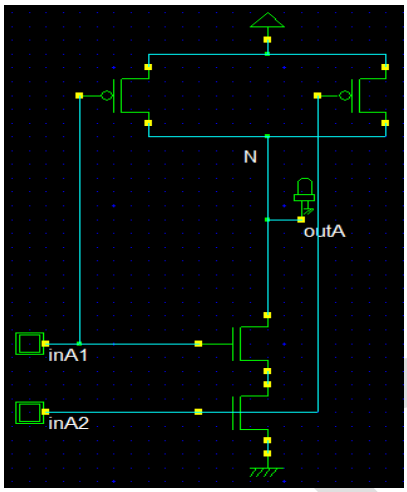

Fig -1: Conventional CMOS NAND Gate Circuit

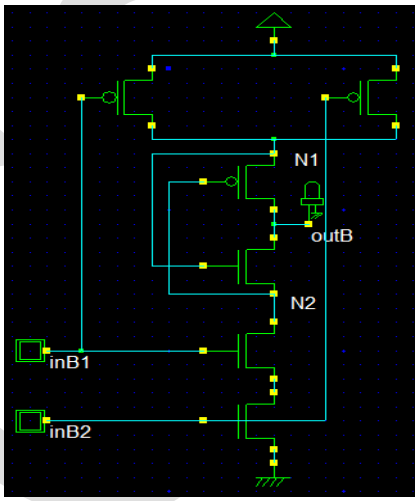

Fig -2: Lector CMOS NAND Gate Circuit

CONVENTIONAL 6-T SRAM MEMORY ARCHITECTURE

The conventional architecture of SRAM Cell has 6-transistors. It is shown in Fig-3. At deep sub-micron scale the leakage power of SRAM circuit is comparatively high as compared to the other operational circuits. The concept of SRAM architecture is based on the stabilization of logic values to maintain its existence against any current or power loss with the ease of data modification using two feedbacks coupled CMOS Inverters. The output terminals of the two inverters act as internal load lines of the SRAM cell to store the memory data bit value on one of the internal load line and its complement logic value on the other internal load line.

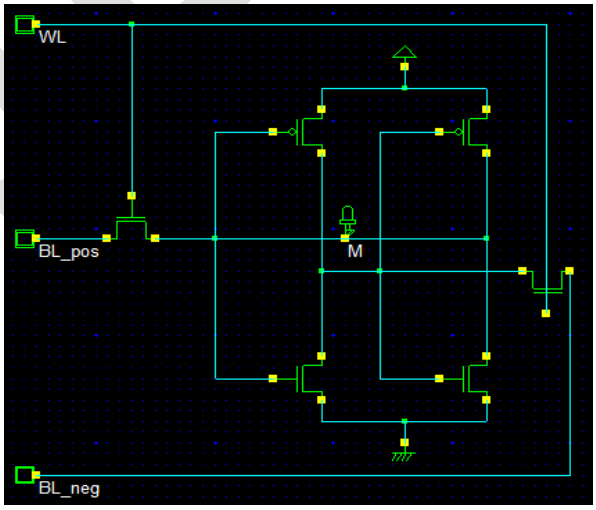

Fig -3: Architecture of SRAM 6-T Cell

Write Operation- The logic data bit to be written in a SRAM cell is provided on the BL_pos and its complement logic value is provided on BL_neg. The WL input is provided a logic high pulse on NMOS data access transistors to enable the transfer of charge from the data lines (BL_pos and BL_neg) to the SRAM cell internal circuit. The duration of pulse should be more than the duration in which the charge on BL_pos and BL_neg should get shared by the SRAM internal load lines to store the desired logic value in the SRAM cell.

Read Operation- To read the data from the SRAM cell, logic high values are set on BL_pos and BL_neg. The WL input is provided a high pulse to enable the sharing of charge between the data lines, BL_pos and BL_neg, and the internal load lines. The data line (BL_pos or BL_neg) connected to the cell internal load line with logic value'1' will not show any change in the logic value after sharing of charge because of the same voltage on both the data lines. Whereas, the other data line will be affected by a small change in its voltage value after sharing the charge with the cell internal load line. Since the current driving capacity of the cell is very low, the change sharing will have a small voltage change effect when logic '0' at the internal load line is shared with the logic '1' of the data line. This voltage difference developed in the load lines is measured using the sense amplifier circuit to know the logic value that is stored in the cell.

PROPOSED SRAM ARCHITECTURE USING LECTOR TECHNIQUE

The architecture of SRAM 6-T cell is the basic architecture for all SRAM architectures. The proposed SRAM architecture of SRAM using leakage control transistors (Lector) technique is shown in Fig-4. The modified design has leakage control transistor pairs connected to the cell internal load lines. The output to the internal load lines is taken from in-between the two transistors of each of the pair of the leakage control transistor. This approach introduces 4-transistors in the existing SRAM architecture. The connection of transistors is shown in Fig-4. The voltage on each of the internal load line will be a constant voltage for a particular memory data in an application, one of the two transistors of the leakage control configuration will remain in its cutoff state leading to a control over the leakage current.

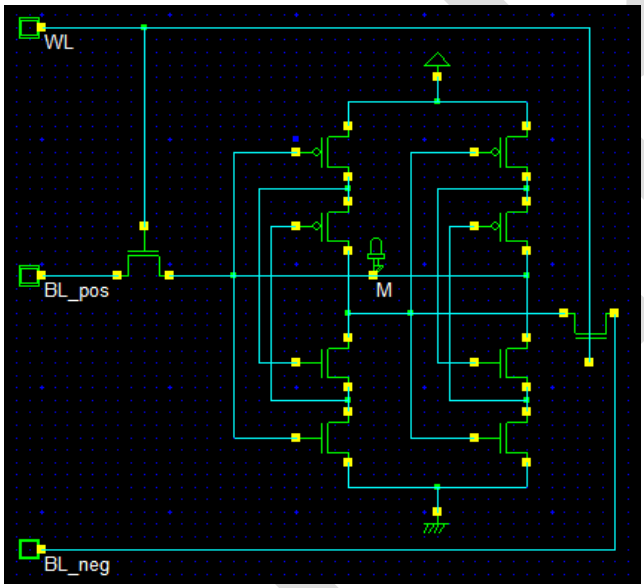

Fig -4: Architecture of SRAM Cell using Lector

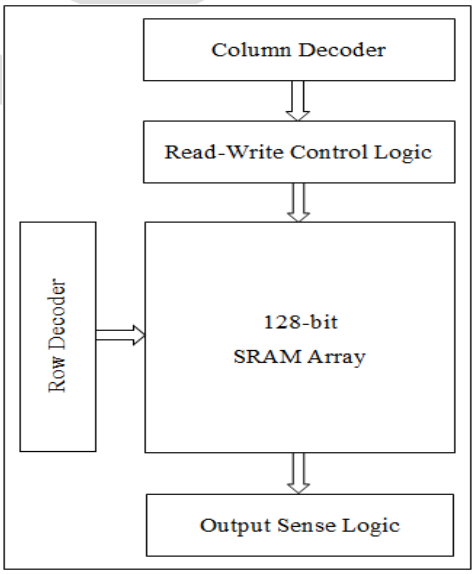

Fig -5: Block Diagram of SRAM Array with control Logic

128-bit SRAM Array: An array of SRAM cells require some additional circuit blocks for its operation. These additional blocks mainly include Row Decoder, Column Decoder, Read-Write Control Logic, Output Sense Logic. The architecture of 128-bit array and control circuit block using Lector is shown in Fig-5.

The Row Decoder logic enables a particular row for performing the operation of data read from array or data write in to the array. A Similar logic is used to enable a particular row or more than one rows to enable a single SRAM cell or multiple cells respectively. Fig-6 shows Row Decoder connection with the 128-bit memory array of the proposed Lector based design. The array has 8x16 bit memory

capacity. The internal circuit connections for desired control of the Row Decoder are shown in Fig-7. The input 'E' is used to enable a particular Row. Inputs A,B,C, represent the 3-bit encoded address. Z1, Z2, …Z8 represent the address lines that are connected to one of the row of the array.

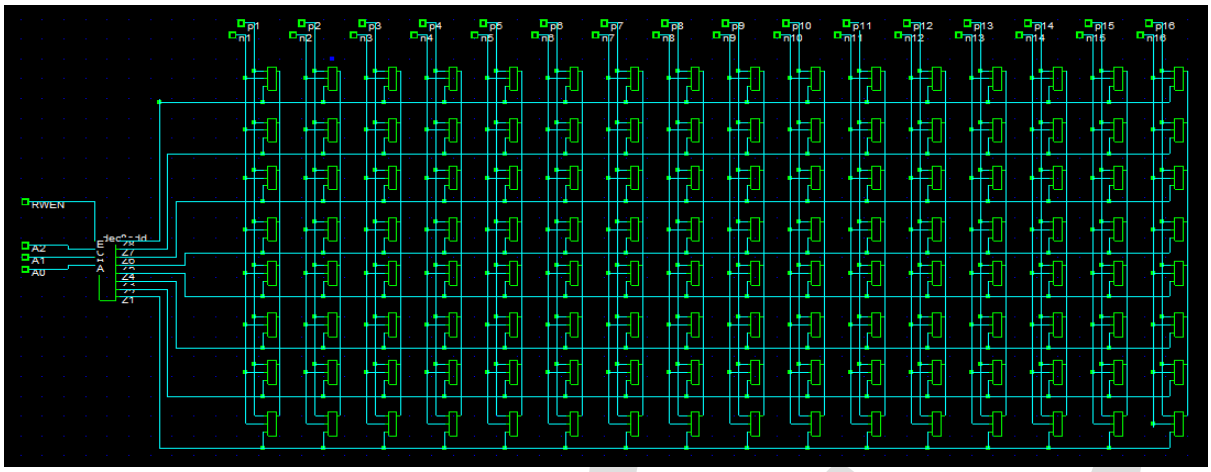

Fig -6: Architecture of SRAM Cell using Lector

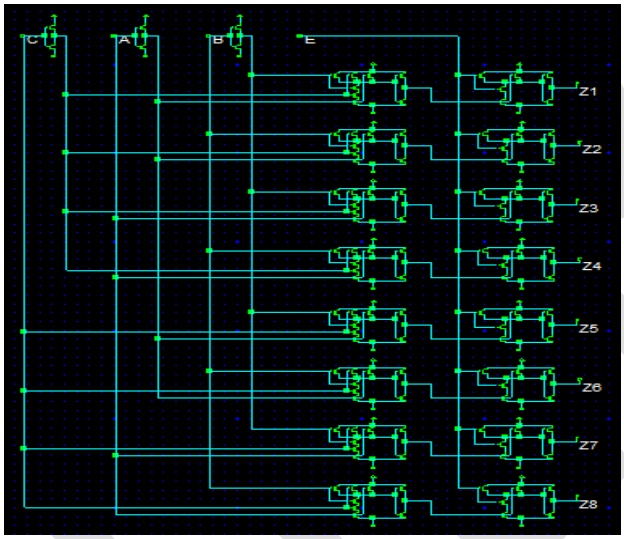

Fig -7: Address Decoder Circuit for 8-Address Length

Address Enable (E)	Address (A B C)	Output (Z1 Z2 Z3 Z4 Z5 Z6 Z7 Z8)
0	X X X	0 0 0 0 0 0 0 0
1	0 0 0	1 0 0 0 0 0 0 0
1	0 0 1	0 1 0 0 0 0 0 0
1	0 1 0	0 0 1 0 0 0 0 0
1	0 1 1	0 0 0 1 0 0 0 0
1	1 0 0	0 0 0 0 1 0 0 0
1	1 0 1	0 0 0 0 0 1 0 0
1	1 1 0	0 0 0 0 0 0 1 0
1	1 1 1	0 0 0 0 0 0 0 1

Table -1: Truth Table of 8-bit Address Decoder

The truth-table of Row Decoder is shown in Table-1. For Enable, E='0', none of the row of the array is enabled for Read / Write operation. For E='1', the address value from the inputs A-B-C is decoded to enable a particular address Row.

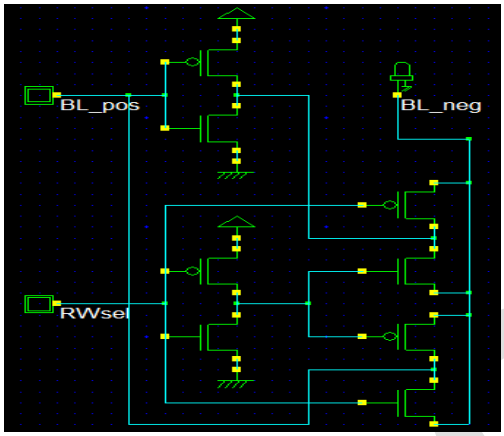

Fig -8: Architecture of Read-Write control Logic Circuit for single column.

The Read-Write Control Logic sets the voltages on the BL_pos and BL_neg load lines to enable the Date Read and Data Write operations depending on the value of the RWsel control input. In the proposed design of Read-Write control logic block, the control logic performs Read operation for RWsel='1' and Write operation for RWsel='0'. The architecture of the Read-Write Control Logic for a single column output is shown in Fig-8.

SIMULATION AND RESULT

The date Read and Write operational waveform result obtained during waveform simulation is shown in Fig-9.

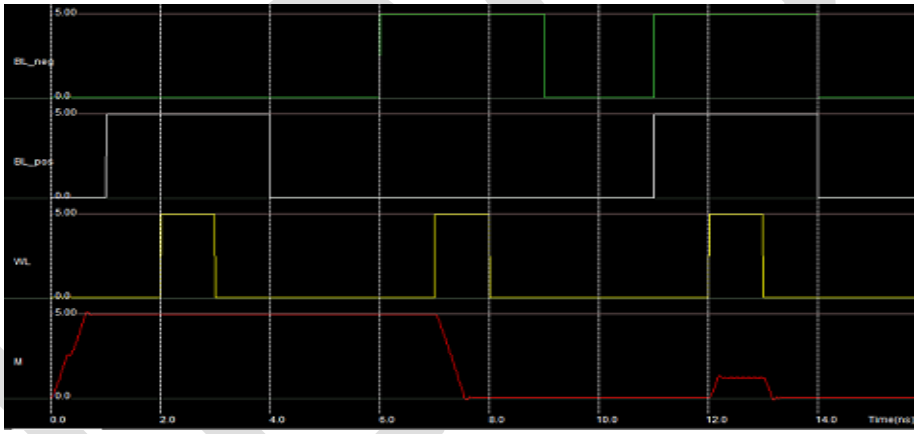

Fig -9: Simulation Waveform of Read-Write Bit operation

The proposed design is simulated using Microwind Tool [18] on multiple deep sub-micron fabrication technologies. The comparison of the proposed design performance with the conventional design is shown in Table-2. Power reduction of the Lector based design at 90nm fabrication technology is ~13%. It can be concluded from the simulation results that the percentage reduction in the power consumption is decreases as simulation is performed towards deep sub-micron technologies.

Technology	Power Consumption		% Decrease in Power
	Conventional design	Lector based design	
50nm	6.416 uW	5.037 uW	22.5
90nm	46.827 uW	40.634 uW	13.3
120nm	73.5 uW	59.73 uW	17.7
180nm	196 uW	103.00 uW	47.5

Table -2: Power Consumption Simulation Result

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CONCLUSION

Memory hardware are very important and mandatory part of all real time processing hardware in the present world of emerging electronic applications. So, a power efficient design is always an expectation of fabrication technology from the hardware designers. The proposed work is an attempt to give an option in the same direction. The area overhead of Lector based design can be compromised with the reduction in power consumption of the SRAM circuit. Further, the existing techniques can be improved in future works in accordance with the day-by-day advancing fabrication methodologies to obtain more improved performance of the memories and other operational circuits.

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