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Comparative Analysis of Low-Power CMOS&DTMOS Full Adder Circuits at 180nm And 45nm Technologies

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ABSTRACT: The full adder circuit is one of the most important components of any digital system application. This paper presents a new low power full adder that uses 8 transistors. The power dissipation, propagation delay and power delay product using 8T full adder are analyzed and Compared with existing techniques 28T,16T,14T,10T transistor full adder designs using HSPICE simulation at 180nm(1.8V) and 45nm(0.7V) technologies. All the circuits are implemented using DTMOS at 45nm (0.3V) technology. Dynamic threshold MOSFET (DTMOS) transistor utilizes dynamic body bias because in DTMOS, substrate (or body) and gate of MOSFET are tied together, therefore the input gate voltage forward biases the source substrate junction and owing to the body effect threshold voltage (V_{th}) decreases in the ON state and when the gate is turned off, V_{th} returns to its original high value in equilibrium. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region.

Key words: CMOS, DTMOS, Full-Adder, low power

I.INTRODUCTION

The explosive growth in laptops and portable systems and in cellular networks has intensified the research efforts in low power microelectronics. In present day there is an ever-increasing number of portable applications requiring low-power and high throughput than ever before. For example note book and laptop computers, representing the fastest growing segment of the computer industry, are demanding the same computation capabilities as found in desktop machines. Therefore, circuits with low-power consumption become the major candidates **[**1] for design of systems. There are several issues related to the full adders. Some of them are power consumption, performance, area, noise immunity and regularity and good driving ability [1]. Several works have been done in order to decrease transistor count and consequently decrease power consumption and area [2]. In some designs, reducing transistor count has been resulted in threshold loss problem that causes non-full swing outputs, low speed and low noise immunity especially when they are used in cascaded fashion. Some of them has threshold loss problem that cause non-full swing outputs and low noise immunity. However, usually they have less power consumption in comparison to full adders with full swing outputs. In Integrated Circuits mainly two types of full adders (Static & dynamic) are used. Static full adders commonly are more reliable, simpler and lower power than dynamic ones. However, dynamic full adders are faster and some times more compact than static full adders. Dynamic full adders suffer from charge sharing, high power due to high switching activity, clock load and complexity.

There are several sources of power consumption in CMOS circuits:

1) Switching Power: Due to output switching during output transitions.

2) Short Circuit Power: Due to the current between VDD and GND during a transistor switching.

3) Static Power: Caused by leakage current and static current.

II. RIPPLE CARRY ADDER

2.1. Designing Ripple Carry Adder

A standard 8-bit ripple-carry adder built as a cascade from eight 1-bit full-adders. C0 for carry-in, inputs are A0..A7 and B0..B7. To demonstrate the typical behavior of the ripple-carry adder, very large gate-delays are used for the gates inside the 1-bit adders - resulting in an addition time of about 0.6 seconds per adder. Note that each stage of the adder has to wait until the previous stage has calculated and propagates its carry output signal. Therefore, the total delay of a ripple-carry adder is proportional to the number of bits. Faster adders are often required for bit widths of 16 or greater.

Each full-adder built by using a new CMOS technology which consumes less power. The PDP exhibited by the full-adder would affect the system's overall performance.

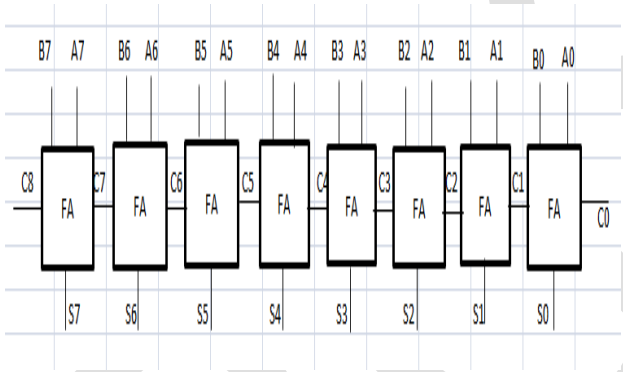

Figure.1 8-bit ripple carry adder

III. RELATED WORK

In the existing method implementation part, The performance analysis and comparison between various parameters that are power, delay, power delay product and rise time ,fall time of different 1-bit and 8-bit CMOS full adders that are 28T,16T,14T,10T are presented here.

The full-adder function can be described as follows: Given the three 1-bit inputs A, B, and C, it is desired to calculate the two 1-bit outputs SUM and COUT, where

SUM = A ⊕ B ⊕ Cin……(1)
Cout= Cin (A ⊕ B) +AB ……(2)

These outputs can be expressed in many different logic expressions. Therefore, many full adder circuits can be designed using the different expressions. There are three main components to design a full adder cell [5]. Those are XOR or XNOR, Carry generator and SUM Generator.

3.1 28T FULL ADDER:

The CMOS design style is not area efficient for complex gates with large fan-ins. Thus, care must be taken when a static logic style is selected to realize a logic function. Pseudo NMOS technique is straightforward. Pass transistor logic style is known to be a popular method for implementing some specific circuits such as multiplexers and XOR-based circuits, like adders.

The conventional CMOS [6] adder cell using 28 transistors based on standard CMOS topology is shown in Fig.2. Due to high number of transistors, its power consumption is high. Large PMOS transistor in pull up network result in high input capacitances, which cause high delay and dynamic power.

However, using inverters on the output nodes decreases the rise-time and fall-time and increases the driving ability. It functions well at low power supply voltages because it does not have threshold loss problem.

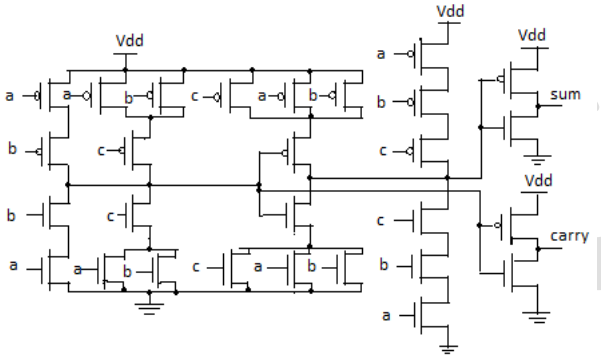

Fig. 2 28T Full Adder

3.2 16T FULL A DDER

The novel adder cell (NEW) has 16 transistor presented here, However, the XOR-XNOR module has been modified to reduce delay and power consumption. Lower power and delay has been obtained at the expense of 2 additional transistors. The novel adder cell (NEW) has 16 transistors. It is based on the 4-transistor implementations of the XOR and XNOR functions pass transistor, and transmission gates. 16T full adder is improved version from 14T, which is called 16T [8]. It has incomplete voltage swing at H when (A = 0, B = 0) and incomplete voltage swing at H' when (A = 1, B = 1) which account for less dynamic power consumption at those nodes. Also, it has less load capacitance at node H, since it is driving fewer loads than all other designs, which provides additional savings in dynamic power.

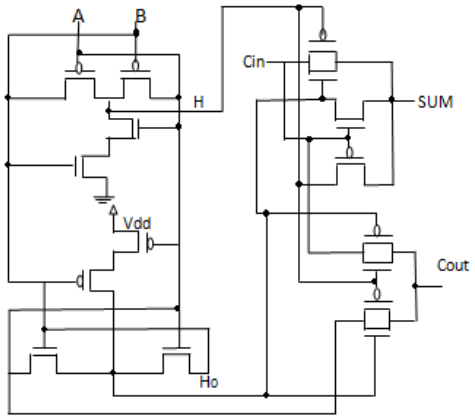

Fig.3 16T full adder

3.3 14T FULL ADDER

One of the recent enhancements is the 14-transistors adder (14T) presented in [10]. Power consumption has been reduced by using the 4-transistor XOR implementation presented in [7], which decreases the overall cell transistor count to 14 (see Fig. 4) .

14T uses only one inverter, but it has the same problem of glitches in the outputs. Also, it has the drawback of introducing a static power component at the inverter output. Due to the incomplete voltage swing of the XOR gate when A = B = 0, both the N and P

transistors will be ON (N is weakly ON), which will lead to drawing current from the power supply although the circuit is in steady state. This drawback increases the power consumed by this cell, but still it remains a good candidate for low power applications due to having only 14 transistors. This circuit has 4 transistor XOR which in the next stage is inverted to produce XNOR. These XOR and XNOR are used simultaneously to generate sum and cout. The signals cin and cin' are multiplexed which can controlled either by (a ⊗ b).

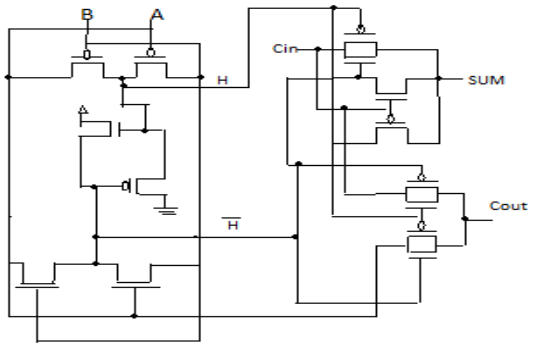

Fig.4 14T full adder

3.4 10T FULL ADDER

SERF (Static Energy Recovery Full Adder) full adder is implemented by 10 transistors, as shown in Fig. 5, uses energy recovery technique to reduce power consumption [8]. SERF use energy recovery technique to decrease the power consumption. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. There are some problems in this circuit. First SUM is generated from two cascaded XNOR gates (group1) which lead to long delay. Second, it cannot work correctly in low voltage. As shown in Fig.6 in the worst case, when A=B='1' there is 2Vtn threshold loss in output voltage. Therefore, logic 1 becomes equal to VDD-2Vtn in this case.

The suitable operating supply voltage is limited to VDD> 2Vtn+|Vtp|. Second, there are five gate capacitances on node X. It causes to long delay in generating of intermediate A⊕ B signal and finally delay in generating SUM and COUT. This problem also increases the power.

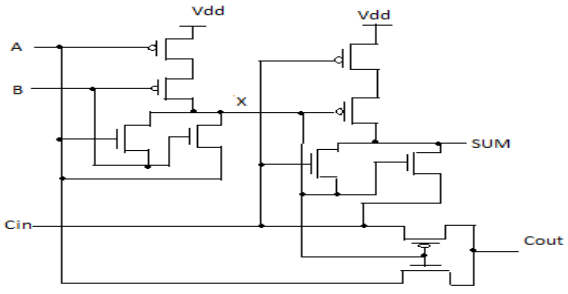

Fig.5 10T full adder

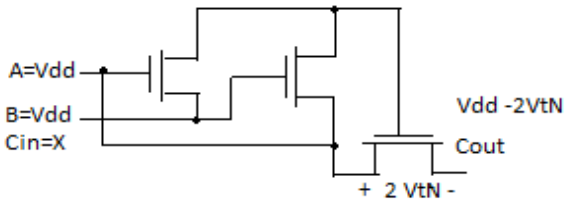

Fig.6 worst case of threshold loss problem in SERF full adder

IV. PROPOSED FULL ADDER

The full adder function can be derived as; the addition of two 1-bit inputs A and B with forestage carry C_{in} calculates the two 1-bit outputs sum and C_{out}, where

Sum = $A \oplus B \oplus C_{in}$……(1)

Cout= C_{in} $(A \oplus B)$ +AB ……..(2)

In this design, the Boolean function as

Sum = $(A \oplus C_{in}) \cdot (C_{out})' + (A \oplus C_{in})' \cdot B$……..(3)

Cout = $(A \oplus C_{in}) \cdot B + (A \oplus C_{in})' \cdot A$……..(4)

From Esq. (3) and (4), the 8T design is proposed (Fig. 7).

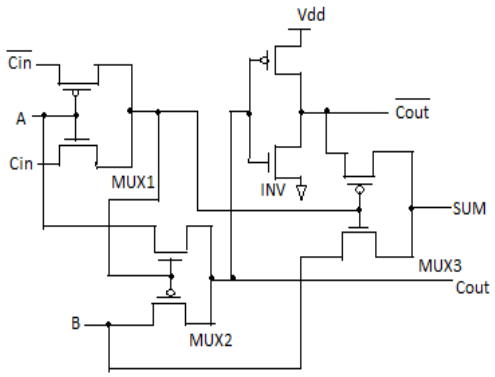

Fig.7 8-transistor full adder

The entire design process can be divided into several steps as follows:

1. $(A \oplus C_{in})'$ or $(A \oplus C_{in})$ is needed as a control signal in multiplexers MUX2 and MUX3 to generate Cout and Sum. $(A \oplus C_{in})'$ is implemented by MUX1 (Fig. 7).

2. The multiplexer circuit MUX2 is adopted in our proposed design to generate Cout followed by an inverter INV. Using inverter in the circuit; it speeds up the carry propagation as a buffer along the carry chain. Secondly, it provides complementary signals needed for the generation of Sum (Lin et al., 2007).

3. The Sum is generated by the multiplexer MUX3 passing either B or out C_{out}' according to the value of in $(A \oplus C_{in})'$.

The proposed full adder circuit, which uses three multiplexers and an inverter, requires eight transistors. Choosing appropriate width to length rates of transistors, W/L, improves the threshold drop of the circuit (Chowdhury et al., 2008). The multiplexer uses transistor sizes of (W/L)p=6/1 and (W/L)n=3/1 for PMOS and NMOS, respectively, while the inverter uses the

typical sizes of (W/L)p=4/1 and (W/L)n=2/1 (Fig. 7). The 8T full adder showed better performance than other full adders due to its low power consumption and propagation delay.

V. SIMULATION RESULTS

All the 1-bit and 8-bit full adders have been simulated at 180nm technology under the voltage V_{DD}=1.8V tabulated in Table 1 and Table 2, and at 45nm technology under the voltage V_{DD}=0.7V tabulated in Table 3 and Table 4.

Table .1 Simulation Results Of All CMOS 1-Bit Full Adder At 180nm Technology

Parameter/ Full Adder	Voltage (V_{DD})	Average power (W)	Propagation delay(S)	Power delay product(J)
28T	1.8V	11.66E-06	12.35E-12	14.40E-17
16T	1.8V	10.78E-06	9.379E-12	10.11E-17
14T	1.8V	9.797E-06	11.35E-12	11.11E-17
10T	1.8V	9.664E-06	10.07E-12	9.727E-17
8T	1.8V	7.812E-06	3.432E-12	2.680E-17

Table .2 Simulation Results Of All CMOS 8-Bit Full Adder At 180nm Technology

Parameter/ Full Adder	Voltage (V_{DD})	Average power (W)	Propagation delay(S)	Power delay product(J)
28T	1.8V	5.484E-05	14.42E-12	7.907E-16
16T	1.8V	4.409E-05	10.42E-12	4.594E-16
14T	1.8V	3.793E-05	13.71E-12	5.200E-16
10T	1.8V	3.746E-05	11.73E-12	4.394E-16
8T	1.8V	3.205E-05	8.957E-12	2.860E-16

Table .3 Simulation Results Of All CMOS 1-Bit Full Adder At 45nm Technology

Parameter/ Full Adder	Voltage (V_{DD})	Average power (W)	Propagation delay(S)	Power delay product(J)
28T	0.7V	4.265E-07	0.898E-12	3.829E-19
16T	0.7V	3.669E-07	0.546E-12	2.003E-19
14T	0.7V	3.157E-07	0.616E-12	1.944E-19
10T	0.7V	2.049E-07	0.592E-12	1.213E-19
8T	0.7V	1.348E-07	0.332E-12	0.447E-19

Table .4 Simulation Results Of All CMOS 8-Bit Full Adder At 45nm Technology

Parameter/ Full Adder	Voltage (V_{DD})	Average power (W)	Propagation delay(S)	Power delay product(J)
28T	0.7V	6.565E-05	5.562E-12	3.651E-16
16T	0.7V	3.525E-05	2.619E-12	0.923E-16
14T	0.7V	3.053E-05	4.171E-12	1.456E-16
10T	0.7V	1.876E-05	3.274E-12	0.614E-16
8T	0.7V	1.571E-05	2.003E-12	0.314E-16

From Table 1, 2 and Table 3, 4, 28T full adder has more power and delay and PDP compared to 16T, 14T, 10T full adders, because more number of transistors results in high input loads, more power consumption. In 16T full adder the XOR-XNOR module has been modified to reduce delay and power consumption. Lower power and delay has been obtained at the expense of 2 additional transistors. 14T full adder has simultaneous XOR and XNOR signals. Feedback transistors provide rail-to-rail outputs in XOR-XNOR module.

However, they prompt high delay than 16T full adder. SERF use energy recovery technique to decrease the power consumption. Energy recovery logics reuse charge. Therefore, it consumes less energy than the other full adders. There are some

problems in this circuit, SUM is generated from two cascaded XNOR gates which lead to long delay, compared to 16T full adder it has more delay. 8T full adder shows a much better power, delay and power delay product (PDP) compared to any other adders mentioned in Tables. Compared to 180nm technology the 45nm technology has low power, delay and power delay product.

VI. COMPARISION OF CMOS AND DTMOS

FULL ADDERS

MOSFET devices are generally operated above threshold voltages but the devices can also exhibit control characteristics, even below the threshold voltages. This region of operation of these devices may be called sub threshold operation.

Dynamic threshold MOSFET (DTMOS) transistor utilizes dynamic body bias because in DTMOS, substrate (or body) and gate of MOSFET are tied together, therefore input gate voltage forward biases the source substrate junction and owing to the body effect threshold voltage (V_{th}) decreases in the ON state and when the gate is turned off, V_{th} returns to its original high value in equilibrium. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region.

6.1 Structure Of CMOS and DTMOS Configuration

Typical schematic structures of CMOS and DTMOS [3] are given in Figure 11.1(a), 11.1(b). In conventional NMOS circuit, Fig. 11.2(a), the substrate is normally connected to ground or lowest potential in the circuit and in PMOS circuits, the substrate is connected to supply voltage (VDD=0.3V) or the highest potential in the circuit. In DTMOS, Fig 11.2 (b), the substrate is always kept at gate potential. Also, the voltage of each transistor substrate is dynamically adjusted depending on the gate voltage, causing the threshold voltage of the device to adjust dynamically. DTMOS devices are efficient because they function as dual threshold logic gates. When a DTMOS transistor is ON, its threshold is lowered increasing the current and decreasing propagation delay. Likewise when the transistor is OFF, the threshold is raised, reducing leakage current and minimizing power and energy dissipation. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region.

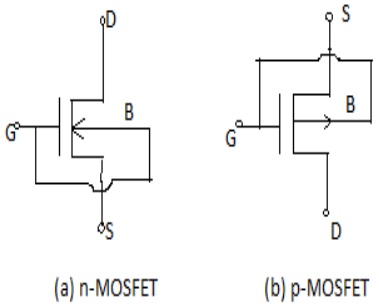

Fig 11.2 - DTMOS Structure

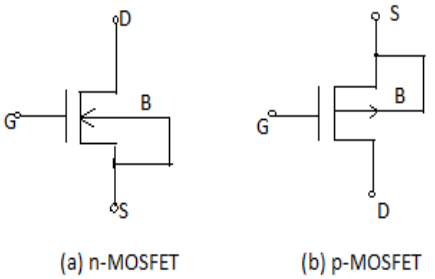

Fig 11.2 - DTMOS Structure

VII .SIMULATION RESULTS

All the 1-bit full adders have been simulated at 45nm technology under the voltage V_{DD}=0.3V and the comparison of CMOS and DTMOS of the results have been tabulated in Table 5.

Table. 5 Comparison Results Of CMOS&DTMOS Of 1-Bit Full Adder At 45nm

Technology (0.3V)

Parameters	Voltage (V_{DD})	full adders	CMOS	DTMOS
Average Power(W)	0.3V	28T	2.609E-07	2.901E-07
		16T	2.196E-07	2.483E-07
		14T	2.143E-07	2.220E-07
		10T	0.675E-07	0.780E-07
		8T	0.102E-07	0.136E-07
Propagation Delay(S)	0.3V	28T	0.704E-12	0.218E-12
		16T	0.393E-12	0.130E-12
		14T	0.635E-12	0.180E-12
		10T	0.444E-12	0.143E-12

		8T	0.207E-12	0.118E-12
Power Delay Product(J)	0.3V	28T	1.838E-19	0.635E-18
		16T	0.863E-19	0.032E-18
		14T	1.362E-19	0.039E-18
		10T	0.299E-19	0.011E-18
		8T	0.021E-19	0.001E-18

From the above Table 5 DTMOS has less delay and power delay product and more power compared to CMOS. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region. Compared to all CMOS and DTMOS full adders, proposed 8T full adder has less power, delay and power delay product. Power consumption less in 8T full adder. Dynamic threshold MOS (DTMOS) circuits provides low leakage and high current drive compared to CMOS circuits, operated at lower voltages. Regarding speed, DTMOS 8T is superior; it is faster than CMOS 8T by 50%.

Table .6 Comparison Results Of CMOS&DTMOS Of 8-Bit Full Adder At 45nm

Technology (0.3V)

Parameters	Voltage (V_{DD})	full adders	CMOS	DT MOS
Average Power(W)	0.3V	28T	4.529E-06	4.589E-06
		16T	2.547E-06	2.603E-06
		14T	2.119E-06	2.241E-06
		10T	1.239E-06	1.922E-06
		8T	0.104E-06	0.919E-06
Propagation Delay(S)	0.3V	28T	0.934E-12	0.522E-12
		16T	0.518E-12	0.202E-12
		14T	0.724E-12	0.233E-12
		10T	0.617E-12	0.217E-12
		8T	0.248E-12	0.146E-12

Power Delay Product(J)	0.3V	28T	4.230E-18	2.396E-17
		16T	1.319E-18	0.052E-17
		14T	1.534E-18	0.068E-17
		10T	0.764E-18	0.041E-17
		8T	0.025E-18	0.013E-17

From the above Table 6 DTMOS has less delay and power delay product and more power compared to CMOS. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region. Compared to all CMOS and DTMOS full adders, proposed 8T full adder has less power, delay and power delay product. Power consumption less in 8T full adder. Dynamic threshold MOS (DTMOS) circuits provide low leakage and high current drive compared to CMOS circuits, operated at lower voltages. 8-bit full adder has more power and delay and PDP compared with 1-bit full adder. Regarding speed, DTMOS 8T is superior; it is faster than CMOS 8T by 50%.

CONCLISIONS

The performance of digital VLSI applications depends largely on the characteristics of the full adder circuits employed in such systems. The full adder design proposed is composed of only eight transistors forming three multiplexers and one inverter to produce complementary carry signals (*C*out and out *C*) and summation signal (Sum). Comparing The proposed design with other existing adders in respect of power consumption, delay, and power delay product, the new design embodies a good many advantages. Power, delay and power delay product (PDP) has also been improved. The comparison shows that the implementation of the full adder would be better at 45nm technology as compared to 180nm technology. DTMOS has less delay and power delay product and more power compared to CMOS. DTMOS is an excellent scheme to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region. In future work, the proposed design will be embedded into multiplier to demonstrate the performance in realistic application. Research is going on to further reduce the power and delay, area of full adders.

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