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Reconfigurable N-Point FFT Processor Design For OFDM System

Sumit Wadekar[1], Laxman P. Thakare, Dr. A.Y. Deshmukh

[1]PG Scholar, Department of Electronics,

[1]G. H. Raisoni College of Engineering, Nagpur,India

[1]Email: sumit.wadekar@gmail.com

Abstract— Under many research works, it has been observed that the multiple input multiple output (MIMO) system can be considered an efficient solution for the high-speed wireless communication. However, the delay spreads in non-flat fading channels abrupt the functioning of MIMO system. In orthogonal frequency division multiplexing (OFDM), the channel impulse response is flat in each sub carrier. Hence, MIMO with OFDM can be used effectively in non flat fading channels. MIMO OFDM system requires many independent baseband processors thereby increasing hardware complexity of the system. So there is a need to reduce the hardware complexity of FFT/IFFT processor. The proposed model uses multipath delay commutator (MDC) architecture to design a reconfigurable N-point FFT processor.

Keywords— Multiple Input Multiple Output, Orthogonal Frequency Division Multiplexing, Multipath Delay Commutator, Fast Fourier Transform processor, Inverse Fast Fourier Transform , Wireless, Communication

INTRODUCTION

OFDM is a special type of multi-carrier transmission where a single data stream is transmitted over a number of lower rate sub-carriers. In high speed digital communication, the OFDM technique is widely used against frequency selective fading and intersymbol interference. It is also used for wideband data communication over mobile radio channels, DAB and DVB.

MIMO system, the wireless communication system with multiple antennas at the transmitter and receiver, has received remarkable attention because of its ability to increase system capacity without expanding the bandwidth.

The use of multiple-input multiple-output (MIMO) signal processing with orthogonal frequency division multiplexing (OFDM) can provide enhanced data rates for the next generation wireless communication systems. But as MIMO-OFDM system transmits multiple data streams, it requires various independent baseband processors. This increases its hardware complexity tremendously when compared with single-input single-output OFDM (SISO OFDM) systems.

A very high data throughput rate is provided by the IEEE 802.11n standard based on the MIMO OFDM system. Since FFT processor is one of the most computationally intensive modules of the OFDM processors, it becomes very important to design a low complexity FFT processor. However, MIMO OFDM system with k transmitting and receiving antennas consists of k OFDM baseband processors. This requires k FFT processors thus increasing the hardware complexity by k times.

In WLAN system, the hardware complexity is a very important component as it is used in non-fixed environment. So it is essential to design an efficient system module to reduce the increasing complexity of the MIMO OFDM system. Therefore the focus should be on FFT processor as it is one of the largest block in MIMO OFDM processor.

In the proposed system, a reconfigurable N-point FFT processor for MIMO OFDM system is designed. The proposed FFT processor is based on MDC architecture and can support variable lengths of FFT operations. Section II presents the work done related to reducing the complexity of the FFT/IFFT processor. Section III presents the methodology for the FFT/IFFT processor. Section IV presents the simulation results of the proposed FFT processor and section V concludes the paper.

RELATED WORK

There are various methods which have been used for designing FFT/IFFT processor for MIMO OFDM system.

An area efficient FFT processor for SDR systems based on MIMO OFDM is proposed [1]. The variable lengths of 64, 128, 512, 1024 and 2048 are supported by the proposed FFT processor. The complexity of the proposed FFT processor is decreased by reducing the number of non trivial multipliers. This is achieved by employing mixed radix and multipath delay commutator architecture. In the process, the system throughput is not sacrificed. The design of the proposed FFT processor is made in hardware description language and it is implemented on Xilinx Virtex 4 FPGA.

The FFT processor proposed in [1] reduces the logic slices by 41.9%, dedicated multipliers by 62.5% and memory size by 39% when compared with the conventional 4 channel R2SDF FFT processor. When compared with 4 channel R2MDC FFT processor, the proposed FFT processor [1] reduces the logic slices by 26.2%, dedicated multipliers by 25% and memory size by 26.8%. Thus the complexity of the FFT processor is reduced tremendously.

The scalable FFT processor architecture for OFDM based communication systems is described [2]. In recent times, different mobile devices can support multiple wireless standards [8] and requires efficient transceiver. Hence, in a communication transceiver, the baseband hardware needs to be scalable and efficient across multiple standards.

Design of FFT hardware is a challenging task while balancing design parameters such as speed, power, area, flexibility and scalability. The research work in [2] proposes a scalable radix-2 N-point novel FFT processor architecture. The architecture design is based on an approach to balance various specified design parameters to meet the requirements of SDR platforms supporting multiple wireless standards. The processor operates at a maximum frequency of 200MHz, uses less than 1% of FPGA device resources [9] and meets the performance requirements of multiple wireless standards.

A 128/64 point fast Fourier transform (FFT)/ inverse FFT processor which is applied in wireless LAN processor based on MIMO OFDM multiplexing is proposed in [3]. The sequences of multiple data is properly dealt with by the mixed radix MDF fast fourier transform architecture. The 64 and 128 point FFT operation is supported by the processor. For simultaneous sequences of data, multiple data rates is also provided [10]. Furthermore, less hardware complexity is needed in the design compared with the traditional four-parallel approach. At the operation clock rate of 40 MHz, the processor can calculate 128-point FFT with four independent data sequences within 3.2 us.

A FFT/IFFT processor which can be applied in WLAN processor based on MIMO OFDM system is proposed [4]. Higher mixed radix FFT algorithm is used to achieve better throughput, low power and less complex multipliers. To design FFT/IFFT processor, the mixed radix architecture of FFT is proposed with reversal of bits. The consumption of power is reduced and the hardware is made less complex by the proposed FFT processor [4].

An area-efficient FFT processor for mobile WiMAX systems is proposed [5]. The variable lengths of 1024, 512, 2048 and 4096 can be supported by the FFT processor due to its scalability. The complexity of the processor is decreased considerably by lowering the non trivial multipliers used along with MDC architecture [11]. HDL was used to design the FFT processor. The size of memory is reduced compared with those of the 4-channel radix-2 MDC (R2MDC) FFT processor by the FFT architecture used.

An energy and area efficient structure and hardware architecture of FFT processor for 4x4 MIMO-OFDM WLAN systems with four transmit and four receive antennas is proposed [6]. Since the basic scheme of MIMO-OFDM system is multiple data transmission, conventional FFT processor for SISO-OFDM system is not suitable for MIMO-OFDM systems. The proposed FFT processor has multi-channel structure to support multiple data paths. Multi-channel structure enables the processing of several FFT operations with a single processor [12]. Also, by the mixed radix algorithm, the number of non-trivial multiplications of the FFT processor is decreased. The proposed FFT processor reduces the logic gates over a 4-channel R4MDC FFT processor. Thus, the proposed FFT processor contributes to the low power and low complexity design of MIMO-OFDM systems.

The FFT processor for applications in MIMO OFDM systems which uses low power and has variable length is presented [7]. The variable length of FFT computation is achieved by mixed radix algorithm [13]. To reduce main memory accesses, cache memory architecture is used. Higher SQNR which is required for QAM signals is also achieved by the proposed FFT /IFFT processor. The computation time and the power dissipation of the processor are decreased.

From the related work, it is observed that reducing the complexity of FFT processor is a high priority task. This can be achieved by using a multipath delay commutator (MDC) architecture.

METHODOLOGY

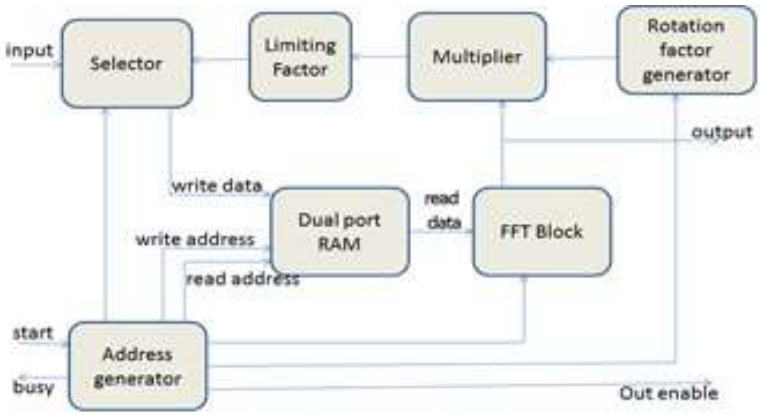

Fig.1 Block diagram of generic N-point FFT

Fast Fourier transformation (FFT) processor is one of the largest modules in the OFDM baseband processor. It is very important to design the low-complexity FFT/IFFT processor for MIMO-OFDM based communication systems. To make FFT processors more area efficient, it is necessary to reduce the parameters of FFT processors like the area, the number of multipliers and the memory size. The proposed model works towards reducing these critical parameters of the FFT processor.

In the proposed system, a generic N- point FFT processor is designed. Radix 4 FFT is used in the design. The various blocks involved in the design of generic N-point FFT is shown in fig.1. FFT points upto 1024 can be calculated using the proposed model. The address generator block generates addresses of the clock. One stage is triggered at a time. Dual port RAM is used as RAM is instantiated two times one for real part and another for imaginary part of the complex number. Radix 4 FFT is used to calculate higher point FFTs upto 1024 point. Inbuilt multipliers (trivial multipliers) are used in the design. The commutator block provides a delay of 1 clock cycle. All the blocks are interconnected to form a generic N-point FFT. The design is simulated on Xilinx ISE 13.2 using VHDL.

RESULTS

The simulation results of generic N-point FFT using radix 4 is shown in fig.2. Iin & Qin are the real and imaginary parts of the complex numbers fed as input to FFT whereas Iout & Qout are the real and imaginary parts of the output of the FFT. The device utilization summary of fig.3 shows the logic utilization of the target device used during the simulation of the FFT processor.

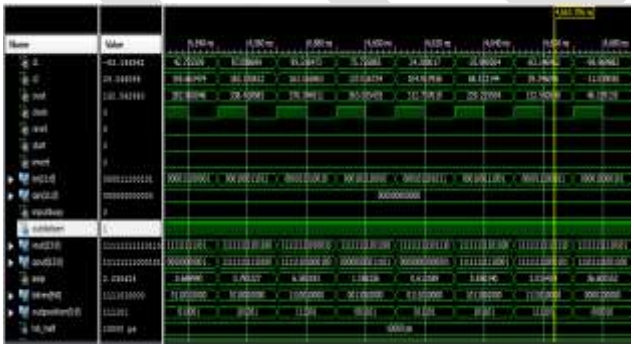

Fig.2 Simulation results of FFT

Device Utilization Summary (estimated values)			
Logic Utilization	Used	Available	Utilization
Number of Slices	506	1920	26%
Number of Slice Flip Flops	799	3840	20%
Number of 4 input LUTs	973	3840	25%
Number of bonded IOBs	64	141	45%
Number of BRAMs	2	12	16%
Number of GCLKs	1	8	12%

Fig.3 Device utilization summary

CONCLUSION

The paper describes the generic model used for the designing of N-point FFT processor for MIMO OFDM system. From the research done and the results observed, it can be concluded that the use of the hardware devices used in the FFT design is optimized.

The simulation results of the design match the calculated results thus verifying the correctness of the design. The FFT processor is reconfigurable and various points of FFT can be calculated using the proposed design.

The future work includes the design of non-trivial multipliers and their use in the design of the FFT/IFFT processor for MIMO OFDM system. The multipliers used in the FFT processor are to be reduced thus reducing the area consumption of the processor.

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