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# Low-Complexity Wallace Multiplier Using Energy-Efficient Full Adder Based On Carbon Nanotube Technology

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**Abstract**— In high speed applications, multipliers and their associated circuits like accumulators, half adders, and full adders consume a significant portion. Therefore, it is necessary to increase their performance as well as size efficiency. In order to reduce the hardware complexity which ultimately reduces an area and power, energy efficient full adders plays crucial role in Wallace tree multiplier. Reduced Complexity Wallace multiplier (RCWM) will have fewer adders than Standard Wallace multiplier (SWM).The Reduced complexity reduction method greatly reduces the number of half adders with 75-80% reduction in an area of half adders than standard Wallace multipliers. In RCWM and SWM, at the last stage Carry Propagating Adder (CPA) is used. This paper proposes use of high speed, low power full adder based on Carbon Nanotube technology in reduced complexity Wallace Multiplier at the place of Conventional Full adder in order to reduce power, area and improvement in speed.

**Keywords**— Wallace Multiplier, energy efficient CNTfull adders, High speed multiplier, CMOS full adder, Carbon Nanotube Field Effect Transistor, High Speed, Low Power

## INTRODUCTION

In digital electronic world, power consumption and delay improvement are the most important parameters of a circuit. Digital signal processing (DSP) and image processing, multiplier play a crucial role. In image processing fast Fourier transform (FFT) is one of the most important transform often used. In Fast Fourier transform, computational process requires large number of multiplication and addition operation. The execution of these algorithms requires dedicated MAC and Arithmetic and Logic Unit (ALU) architectures. Multipliers and adders are the key element of these arithmetic units [9]as they lie in the critical path. Many researchers have tried to implement increasingly efficient multiplier. They aim at offering low complexity, low power consumption and high speed. One such multiplier is Standard Wallace Multiplier (SWM) [3]. SWM is fully parallel version of the multiplier, the carry save adders (CSA) used in SWM are conventional full adders whose carries are not connected. SWM also uses half adders in reduction phase. Reduced complexity Wallace multiplier (RCWM) [1] reduced number of half adders used in SWM with a slight increase in full adders to reduce the number of gates. Both the multipliers SWM and RCWM have same number of stages and delay is also same. The complementary CMOS and CPL designs are two conventional Adders based on CMOS structure. Based on transmission function and transmission gate, TFA and TGA designs were implemented. The other designs are classified as Hybrid designs. This paper proposes use of high speed, low power full adder based on Carbon Nanotube technology (CNT)[4] in reduced complexity Wallace multiplier at the place of carry propagating adder in order to reduce power, area and improvement in speed.

## CARBON NANOTUBE FIELD EFFECT TRANSISTORS (CNFETS)

Carbon nanotube field effect transistor (CNTFET) uses CNT as their semiconducting channels. A single-wall CNT (SWCNT) consists of one cylinder only, and the simple manufacturing process of this device makes it very promising for alternative to MOSFET. The gate-to-source voltage that generates the same reference current is taken as the threshold voltage for the transistor that has different chirality. CNTFETs provide a unique opportunity to control threshold voltage by changing the diameter of the CNT or the chirality vector.

Fig. 1 shows the threshold voltage of both P-CNTFET and N-CNTFET obtained from simulation for various chirality vectors (various n for m = 0) [11].The CNTFETs are particularly attractive due to possibility of near ballistic channel transport, easy application of high–k gate insulator and novel device physics. Although most of the work on CNTFETs has concentrated so far on their d.c. properties, the a.c. properties are technologically most relevant. Theoretically, it is predicted that a short nanotube operating in the ballistic regime, and the quantum capacitance limit should be able to provide gain in the THz range [12].

Comparison of CNTFET-based logic circuits to CMOS logic circuits is necessary to establish means of evaluation for performance metrics such as current density, device switching speed, propagation delay through the gates, switching energy, operating temperature, and cost. However, the technology is not sufficiently mature to enable meaningful comparisons as the positioning techniques must still evolve to enable high-yield volume manufacturing and contact technology must be improved to reduce the impact of contacts on circuit performance.

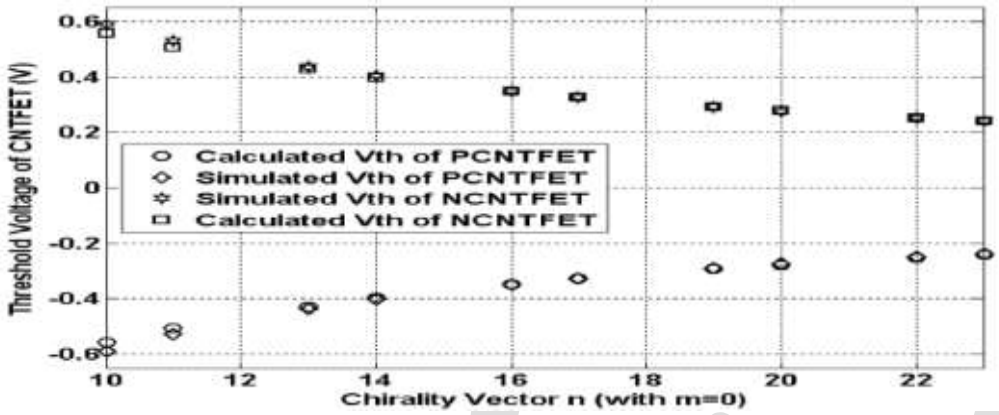


Fig1: Threshold voltage of CNTFETs versus n (for m = 0) [11]

## TRADITIONAL METHOD

### A. Wallace Multiplier

A Wallace Multiplier is an efficient methodology, easily hardware implementable that multiplies two integers, devised by an Australian Computer Scientist Chris Wallace. For unsigned multiplication, up to n shifted copies of the multiplicand are added to form the result. The entire procedure is carried out into three steps: partial product (PP) generation, partial product grouping & reduction, and final addition. The principle of Wallace tree multiplication [3] is shown in Fig. 2. It is clear from the figure that for an n x n multiplication there are $n^2$ partial products that have to be summed. The 1st step in the algorithm involves grouping the partial products into sets of 3. For example, if there are _n' rows of partial products, 3*[n/3] rows are grouped and the remaining n mod 3 rows are passed to the next stage. Therefore in the Fig. 1, three rows of partial products are grouped together in stage 1. These 3 rows are summed using full adders and if there are 2 dots in a particular column half adders are used. The resulting sum and carry signals from the half and full adders are passed to the next stage. The process is repeated till the entire n partial products are summed. The resulting sum and carry out of the last stage is added using a fast carry propagation adder at the final stage.

### B. Reduced Complexity Wallace Multiplier

Reduced complexity Wallace Multiplier (RCWM) is the modified version of Standard Wallace Multiplier (SWM). In SWM they use full adder and half adder in their reduction phase, but half adder do not reduced the number of partial bit , therefore RCWM reduced the number of half adder used in the SWM with slightly increase in full adder .

The partial products are formed by $N^2$ AND gates. The partial products are arranged in a Tree structure format. The modified Wallace reduction method divides the matrix into three row groups. Full adders are use for each group of three bits in a column like the Standard Wallace reduction. A group of two bits in a column is not processed, that is, it is passed on to the next stage (in contrast to Standard Wallace method). Single bits are passed on to the next stage as in the Standard Wallace reduction. The only time half adders are used is to ensure that the number of stages does not exceed that of a Standard Wallace multiplier. For some cases, half adders are only used in the final stage of reduction. In RCWM they uses carry propagating adder (CPA). One possible carry propagating adder for RCWM is a hybrid adder consisting of S+1 ripple carry half adder

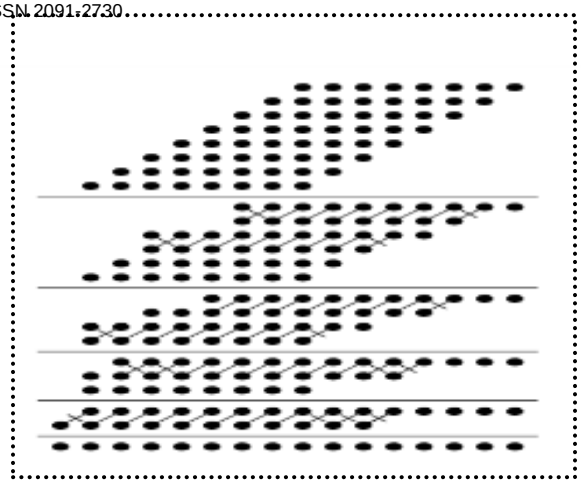

Fig 2. Dot notation for SWM (8 bit) [6]

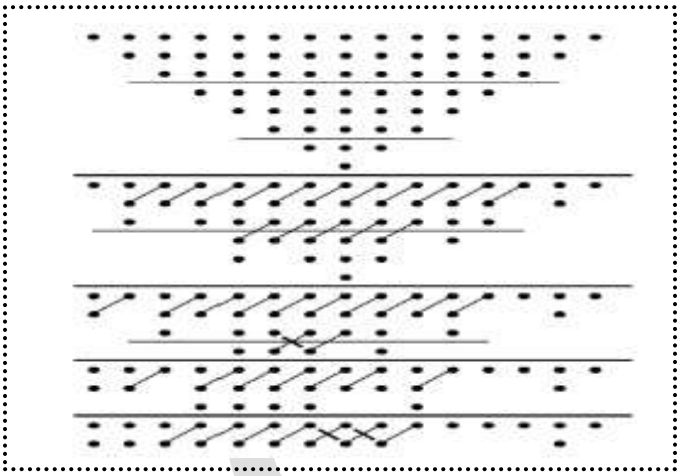

Fig 3. Dot notation for RCWM (8 bit) [6]

## ENERGY EFFICIENT CNT FULL ADDER

Adders are the heart of multiplier. Hence, efficiency of Adders affects performance of multiplier. The conventional adder design depending on input values can have threshold losing in output voltages and are not full swing. For solving this problem, some method such as using transmission gate instead of pass transistor or using output buffers, but these methods cause to increase transistor using and critical path and in result increasing power consumption and delay. CNFETs have a special property that can be used for this case[4]. The threshold voltage is inversely proportional to the diameter of its CNT. So by increasing the diameter of CNT, $V_{th}$ can be reduced. Decreasing of $V_{th}$ leads to better driving capability and higher speed and the full swing problem can be solved

**Design of a Energy Efficient CNT Full Adder**

The logic formula for a one-bit full adder is shown in Equation (3). The inputs are A, B, C (C is carry input) and outputs are Sum and Cout.

$$SUM = XOR(A,B,C) = A \oplus B \oplus C \qquad (1)$$

$$= (A \oplus B) \oplus C$$

The Sum is generated by using XOR twice. First, A and B become XOR and then the result of previous stage become XOR with C. A XOR module is illustrated in Figure 4. This module uses two pass transistors and two pull down transistors. Pass transistors can cover the 3 states of inputs that are 00, 01, 10 and one more remained state (11) is handled by pull down network.

In this design to implement Cout Equation NCNFET and a PCNFET pass transistor are used

$$Cout = C(A \oplus B) + AB$$

$$= C(A \oplus B) + A\overline{A}\overline{B} + AAB \qquad (2)$$

$$= C(A \oplus B) + A(\overline{A}\overline{B} + AB)$$

$$= C(A \oplus B) + A(\overline{A \oplus B})$$

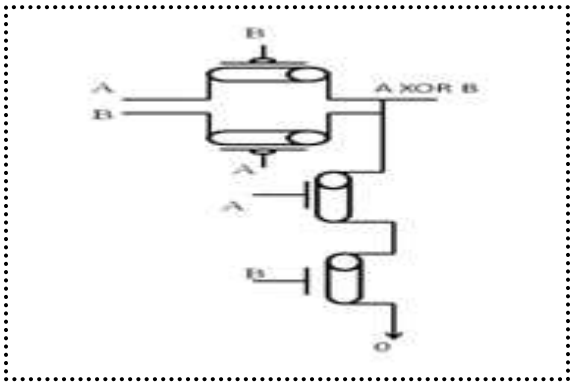


Fig 4. .Design of XOR [4].

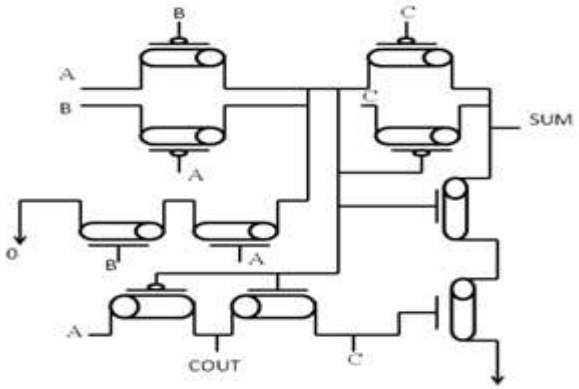


Fig 5. .Design of Full Adder [4].

## PROPOSED ARCHITECTURE

Proposed architecture has same stages as RCW Multiplier. At the stage where conventional full adder is present, Energy Efficient Full Adder is used as shown in Fig 7. Our proposed architecture aims to reduced overall power consumption and leads to increase speed. The design makes use of Energy Efficient CNT Full Adder in Place of conventional full adder. Let two numbers multiply using RCW Multiplier as shown below. The RCW Multiplier has three steps. Multiply (that is - AND) each bit of one of the arguments, by each bit of the other, giving $n^2$ results. Depending on position of the multiplied bits, the wires carry different weights, for example wire of bit carrying result of a2 b3 is 32. Fig 6 shows the multiplication of two 4-bit numbers. The numbers are denoted by A and B where a0 , a1, a2, a3 represents the bits of multiplicand A with as its least significant bit and as its most significant bit and b0, b1, b2, b3 represents the bits of multiplier B with as its least significant bit and as its most significant bit. The Multiplication of the two 4-bit numbers giving partial product which, arrange these partial product bit in tree format and reduced the group two bit using Half adder shown in first stage, and reduced the group of three bit using full adder shown in second stage as of Fig 7. Then final adder adds all the result of second stage and gives final product, which is of 8-bit.

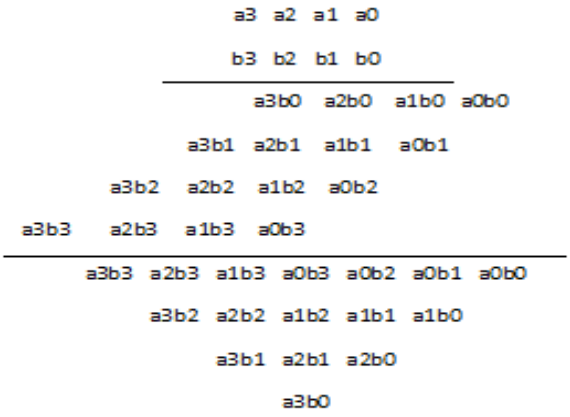


Fig 6. Multiplication of two 4 bit numbers

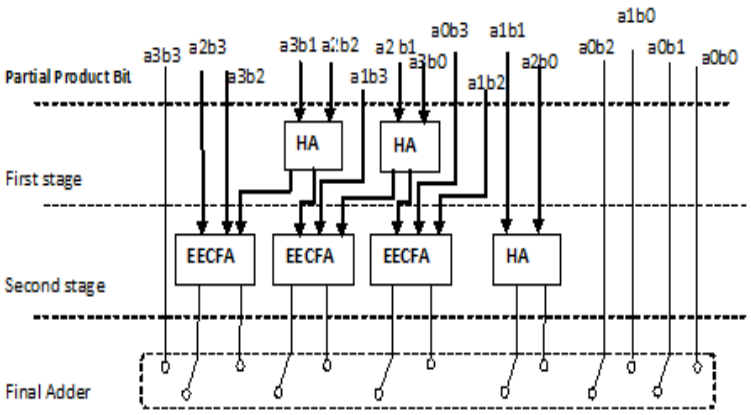


Fig7.Proposed Architecture Of 4×4 Wallace Multiplier

# AREA OPTIMIZED WALLACE TREE MULTIPLIER

TABLE I. Complexity of Reduction

| | Proposed Wallace Tree Multiplier using EECNTFA | | | | | |
|---|---|---|---|---|---|---|
| Number of bits | 4 | 8 | 16 | 24 | 32 | 64 |
| Number of stages | 2 | 4 | 6 | 7 | 8 | 10 |
| Full Adders | 12 | 39 | 201 | 490 | 907 | 3853 |
| Half Adders | - | 3 | 9 | 16 | 23 | 53 |
| Total Gates | 120 | 405 | 2055 | 4980 | 9185 | 38795 |

TABLE II. Comparison table for Full Adder

| ADDER | GATE COUNT |
|---|---|
| Conventional CMOS Full Adder | 40 |
| Carry Propagate Adder | 32 |
| Energy Efficient Full Adder [4] | 10 |

## SIMULATIO N RESULTS AND ANALYSIS

The simulation was done using 0.18µm technology with length and width specification as given NMOS: L=180nm And W =360nm; PMOS: L=180nm and W=720nm. The convention of the W/L ratio of PMOS being thrice that of NMOS has been adhered to for better results.

### A. Schematic of inverter

Fig. below shows a CMOs inverter using one nMOS transistor and one pMOS. When the input A is 0, the nMOS transistor is OFF and the pMOS transistor is ON.

### B. Result of CMOS inverter

This section analyzes the static and dynamic power of an inverter Design with 0.25 µm technology. Static power comes to be 2 m and dynamic power comes to 18 mw as shown in Fig 8.

Fig 8. Wave form for Inverter

## CONCLUSION

This paper proposed an improvement of reduced complexity Wallace Multiplier with reduced power consumption and area by using Energy Efficient CNTfull adder at the place of conventional Full adder. From the literature view it can be inferred that proposed multiplier reduced power and total gate count i.e. reduced area.

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