International Journal of Engineering Research and General Science Volume 3, Issue 2, Part 2, March-April, 2015
ISSN 2091-2730

Performance of 14nm SOI FinFET with ZrO_2 dielectric: A Comparative Study

PushpaK[1], Dr.Kiran Bailey[2], Sowmya Sunkara[3]

[1]M.Tech student, BMSCE, Bangalore

[2]Asst.Professor, Department of ECE, BMSCE, Bangalore

[3]Asst.Professor, Department of ECE, BMSCE, Bangalore

Email:- pushpaachar@gmail.com

Abstract— In this work the High-K dielectric material Zirconium Dioxide (ZrO_2) has been used as the gate oxide in 14nm SOI FinFET structure. The Sentaurus TCAD simulations are used to examine the impact of a High-K gate dielectric on the device short channel performance and scalability of nanoscaleTrigateFinFET. The simulations performed on the device shows that gate leakage is significantly reduced which results in further possible device scale down. The device performance is compared with the conventional structure in which SiO_2 is used as dielectric material. The process variability analysis has been done on both the structures.

Keywords— Zirconium dioxide, SOI FinFET, High K dielectric, gate leakage, TCAD, Process variability, DoE.

INTRODUCTION

Over the past few decades it has been attempted to reduce the size of transistors on the basis of Moore's Law, which states that the number of transistors per chip doubles every 18 months. But this reduction in the transistor dimensions is obstructed by the short-channel effects. TheFinFETS are the promising candidates to replace conventional planar MOSFETs[1]. The leakage current of the device has been increasing with the continuous device scaling resulting on a huge increase in static power dissipation which became a significant portion of the power dissipation in CMOS circuits. Therefore High-*K* is needed to replace SiO_2 to reduce the gate leakage current, thus reducing the static power dissipation. Different types of High-K materials are barium strontium titanate (BST), tantalum oxide (Ta2O5), titanium oxide (TiO2), hafnium oxide (HfO2), zirconium oxide (ZrO2), silicon nitride (Si3N4) and aluminium oxide (Al2O3). The problems in selecting High K include defects in the material that lead to undesired transport through the dielectrics and trapping-induced instabilities.These problems can be minimized by inserting a thin SiO_2 interfacial layer between the silicon substrate and the High-K Dielectric [2]. The earlier studies show that Hafnium based and Zirconium based materials are compatible with Silicon.The novel material ZrO2 has a dielectric constant of 23[4].

FINFET STRUCTURE

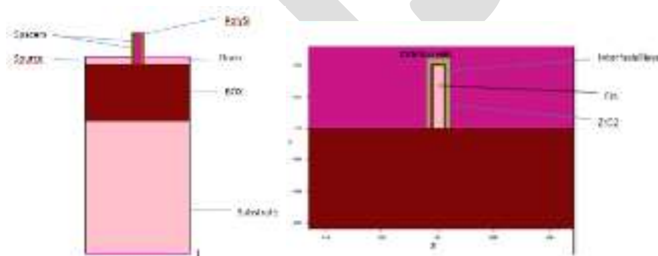

Fig. 1.Schematic showing the 3-D FinFET

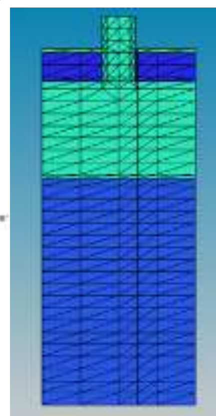

Fig. 2. Meshing in Sentaurus Structure Editor

Fig.1 shows the structure of 14nm SOI FinFET created using Sentaurus TCAD tool. Fig.2 is the meshing of the device, to apply suitable physical models and corresponding current equations on the device.

Table 1 Device Design Specifications

Parameters	Values
Length of the gate (Lg)	14nm
EOT	0.82nm
Thickness of fin (Tfin)	4nm
Doping Concentration of source and drain (cm^{-3})	1e+20
Doping Concentration for Channel(cm^{-3})	1e+16
Dielectrics Used	SiO_2,ZrO_2

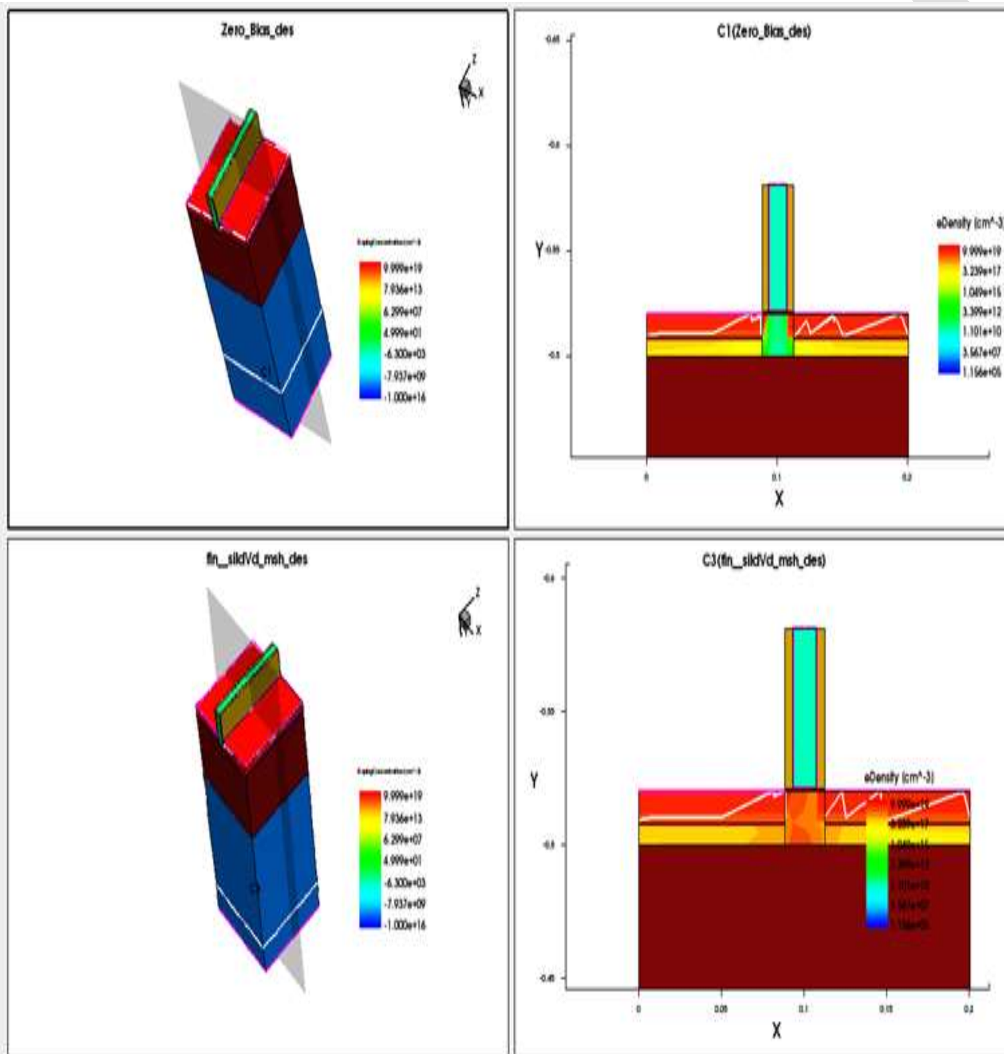

Fig. 3. Electron Density in channel at Vg=0v and at Vg=0.8

Fig.3 shows how channel is formed below the gate for Vg=0.8V(Electron Density)

RESULTS AND DISCUSSION

DC Analysis

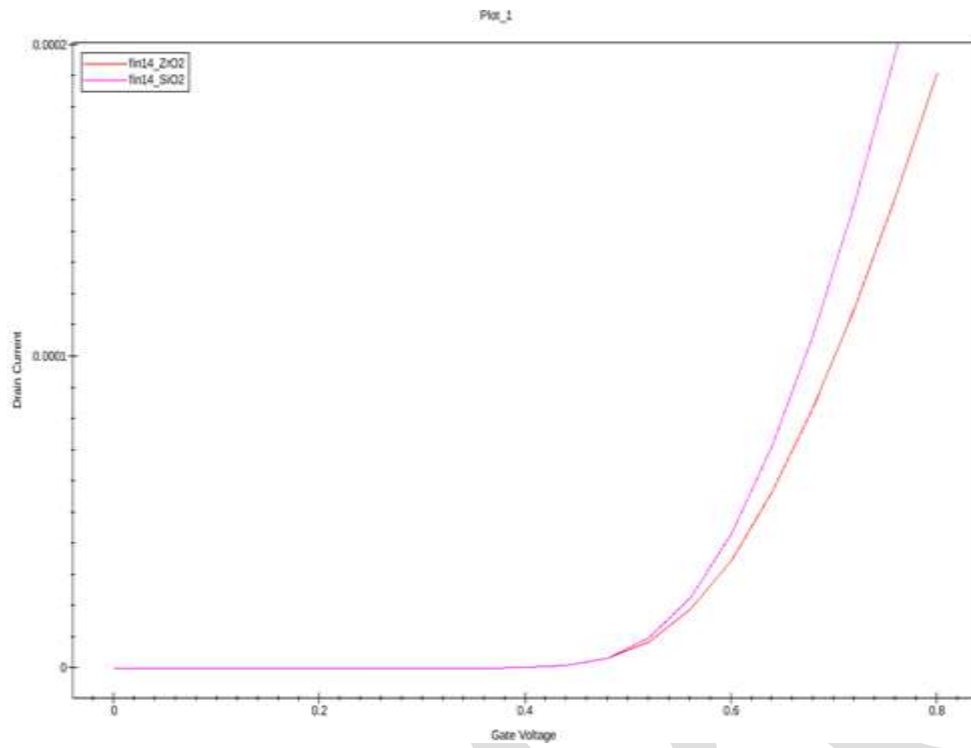

Fig. 4. Id –Vg Characteristics

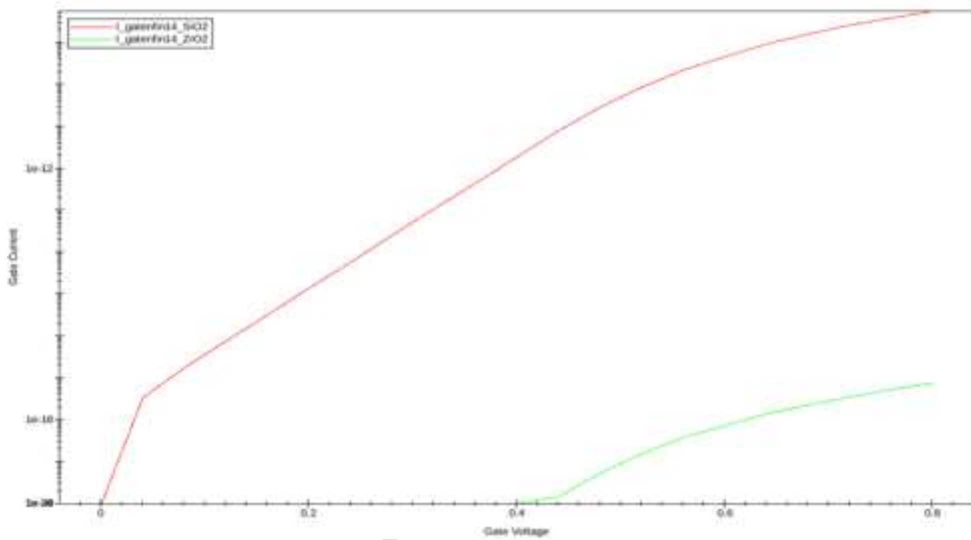

Fig. 5. Gate leakage current Vs Gate voltage

Small Signal AC Analysis

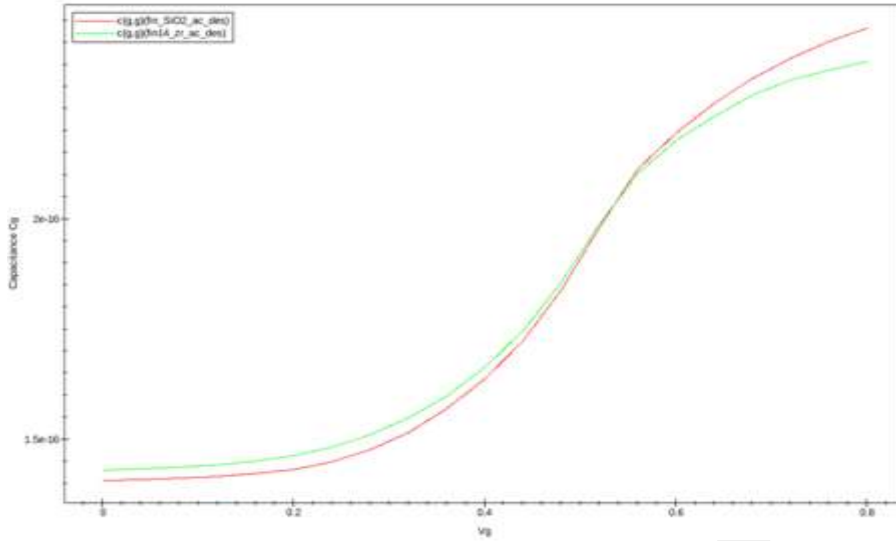

Fig. 6.Capacitance Curve

The characteristics of these devices can be plotted using svisual or inspect.Fig.4 Id vs Vg and Fig.5 IgVs Vg are the results of DC analysis in which both ZrO2 as well as SiO2 dielectric FinFETs are compared. Another important AC characteristic which gives Gate capacitance is shown in the Fig.6 .

Table 2.Comparison of Results

	Gate Oxide	
FinFET	**SiO2**	**ZrO2**
Threshold Voltage(V)	0.604528	0.598723
Gmax	0.001272	0.000941
Ion(A)	0.0002514	0.0001912
Rout(Ω)	9.56E+07	8.01E+07
Ron(Ω)	0.747161	1.01684
DIBL	0.0240247	0.026483
SS(mV/dec)	64.118	65.135
Ioff(A)	1.2299E-13	1.4846E-13
Gate Leakage Current(A)	5.67E-09	7.70E-18

3.3 Process Variability Analysis

Process variation is quite natural in the attributes of transistors when integrated circuits are fabricated. It becomes especially important at smaller process nodes (<60nm). In this work Channel length, Width of the Fin, Oxide thickness, Height of the Fin and Channel doping are the process parameters. The variations will strongly impact the performance metrics of a circuit, such as delay, dynamic power and static power consumptions, which may exhibit greater variability leading to the degradation of yield, increased cost and time to market in modern technologies and their applications.

TABLE 3. Geometric Corner Values of Process Variations For Process Parameters

Process parameters	Nominal Values	Deviation from the nominal values[4]	Range of values(in nm)
L_g	14	10%	12.6 – 15.4
W_{fin}	4	20%	3.2 – 4.8
T_{ox}	0.82	10%	0.738 –0.902
H_{fin}	20	12%	17.6 – 22.4
$N_{ch}(cm^{-3})$	$1x10^{16}$	10%	$0.9x10^{16}$ -$1.1x10^{16}$

3.4 Design of Experiments

A systematic method for experiment planning is used in this technique in order to conduct the experiments in an efficient way and help construct empirical models from which the output responses can be determined as a function of the input factors or parameters.

3.4.1 *Full factorial design*

Full factorial design is one of the most basic techniques in experimental design. In this method, all of the possible combinations of the main parameters or factors and their interactions are considered. Two-level factorial designs are the most widely used method for modelling main effects and interactions as they need a smaller number of experimental runs compared to higher order factorial designs.

In this work, the 5 factors are gate length, width of the fin, Oxide thickness, height of the fin and channel doping. Therefore the total number of experiments equal to 32.The following Table.3 shows the result analysis of 2 level full factorial designs on device responses.

The TABLE.4 shows that the variation of Length of the channel, Oxide thickness and Width of the fin affect more on the performance of the devices.

TABLE 4. Results of Full Factorial Design Analysis

Parameters	Dielectric		Variance
	SiO_2	ZrO_2	
Vth(V)	0.61 +1.701E-3*A +4.367E-3*B -1.165E-3*C	0.6 +1.535E-3*A -2.137E-3*B -1.515E-3*C	*Effect of variation of Lg and W_{fin} on Vth is more in SiO2 than ZrO2 dielectric. * Effect of variation of Tox on Vth is less in SiO2 than ZrO2 dielectric.
Ion(A)	2.565E-4 -1.0512E-5*A +2.22E-5*B -1.084E-5*C	2.35E-4 -2.757E-5*B -1.1E-5*C	*Effect of variation of Lg on Ion is more in SiO2. *Effect of variation of Wfin and Tox on Ion is more in ZrO2
DIBL	0.024 -1.537E-3*A +2.775E-3*B +1.21E-3*C	0.027 -1.638E-3*A +2.937E-3*B +2.812E-3*C	*Effect of variation of Lg,Wfin and Tox on DIBL is more in ZrO2
SS(mV/dec)	64.17 -0.34*A +0.53*B +0.29*C	65.30 -0.44*A +0.53*B +0.66*C	*Effect of variation of Lg and Tox is more on SS in ZrO2
Gate Leakage(A)	gate leakage = +2.082E-008 +1.319E-008 * A -1.173E-008 * B -1.917E-008 * C +1.397E-008 * D -1.245E-008 * AB -1.306E-008 * AC +1.263E-008 * AD +1.191E-008 * BC -1.207E-008 * BD -1.380E-008 * CD +1.246E-008 * ABC -1.248E-008 * ABD -1.262E-008 * ACD +1.209E-008 * BCD +1.248E-008 * ABCD	Sqrt(Gate leakage) = +3.623E-008 +1.579E-009 *A -3.609E-008 * C +2.109E-009 * D -1.573E-009 *AC -2.100E-009 *CD	*Effect of Variation of all the factors(except channel doping) on gate leakage is more in SiO2 *Gate length is less effective in ZrO2 *Effect of interactions also less in ZrO2
Ioff(A)	Ioff = +1.415E-013 -3.283E-014 * A +6.291E-014 * B	Ioff = +1.825E-013 -4.777E-014 * A	*Ioff is affected more by variation of Lg in ZrO2. *Changes in Wfin will not affect much on Ioff in ZrO2

The below Figures shows the performance dependency on the 3 important factors A-channel length, B-width of the fin and Oxide thickness C-Tox .

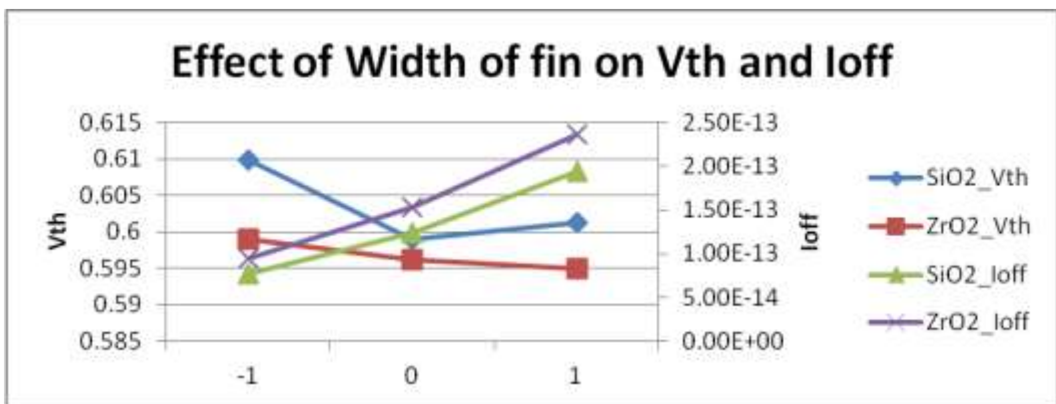

Fig.7.Width vs Vth and Ioff

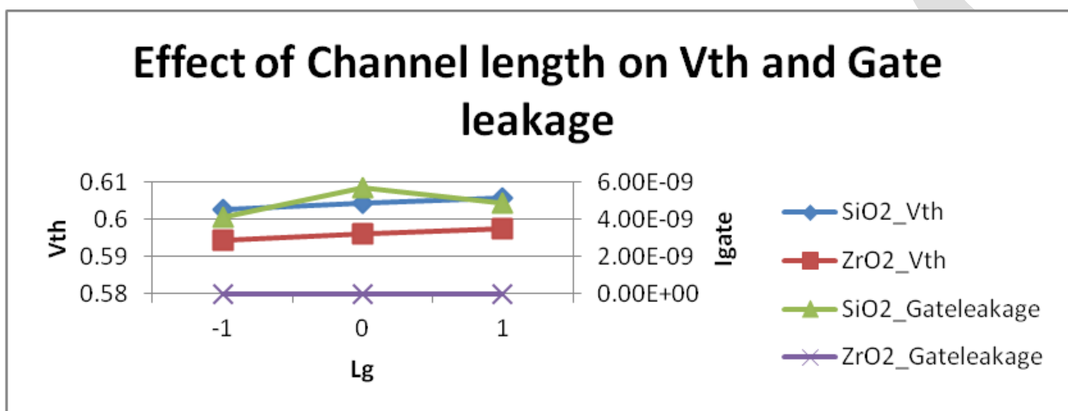

Fig.8.Channel length vs Vth and Igate

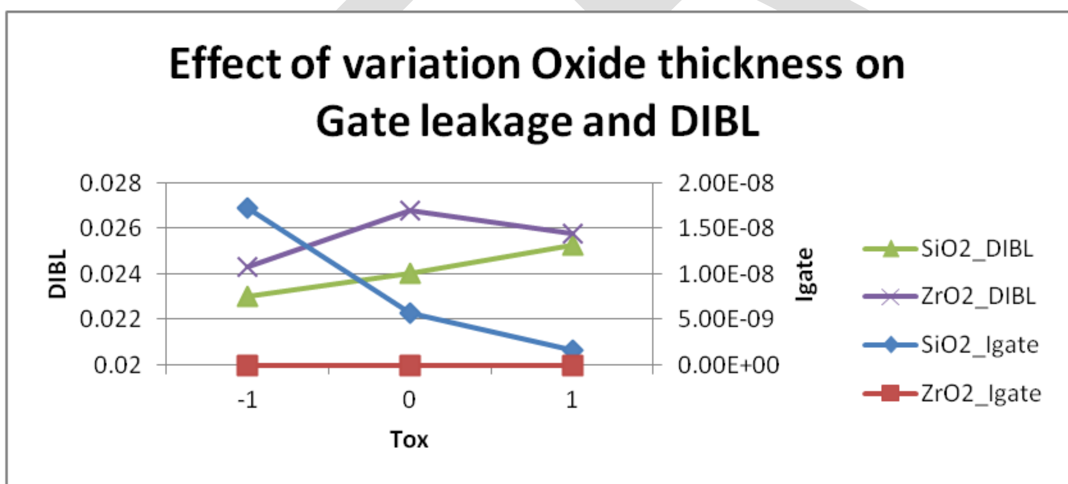

Fig.9.Channel length vs Vth and Igate

Acknowledgment

The authors wish to acknowledge the support of BMS college of Engineering in providing TCAD tool to make the simulation possible.

CONCLUSION

The above analysis shows that effect of variation of channel length on Vth, Ion and gate leakage in ZrO2 dielectric is less compared to SiO2 dielectric. Similarly the effect of width of the fin will not affect the responses Ioff , gate leakage and Vth much in ZrO2. The overall conclusion of the work is the use of High K material ZrO2 reduces the gate leakage current considerably with less variance effect on the responses like Vth, Ion and Gate leakage of the device. This work can be used for further device scale down.

REFERENCES:

[1] DighHisamoto, Wen-Chin Lee, JakubKedzierski, Hideki Takeuchi, Kazuya Asano, Charles Kuo, Erik Anderson, Tsu-Jae King, Jeffrey Bokor, Chenming Hu,"A Self-Aligned Double-Gate MOSFET Scalable to 20 nm" *IEEE Trans. Electron Devices*, vol. 48, pp. 2861–2869, Dec. 2001.

[2] G.Ribes, J. Mitard, M. Denais, S. Bruyere, F. Monsieur, C. Parthasarathy, E. Vincent, and G. Ghibaudo," Review on High-k Dielectrics Reliability Issues," *IEEE Trans. Electron Devices*,and reliability.vol.5, no.1, march 2005.

[3] NagaratnaShanbhag, Kiran Bailey, Dr. K.S. Gurumurthy,"Process Variability Analysis in 14-nm SOI FinFETInverters,"International Journal ofScience,Engineering and Technology Research (IJSETR), Volume 3, Issue 5, May 2014.

[4] D. Nirmal and P. VijayaKumar,"Fin Field effect Transistors Performance in Analog and RF for High-k Dielectrics," Defence Science Journal, Vol. 61, No. 3, pp. 235-240,May 2011.

[5] International Technology Roadmap for Semiconductors, 2012 updates.

[6] Lucian Shifren et al., "Predictive Simulation and Benchmarking of Si and GepMOSFinFETs for Future CMOS Technology", IEEE Transaction on Electron Devices, vol. 61, no. 7, July 2014.

[7] S.mittal et al., "Epi Defined (ED) FinFET: An alternate device architecture for high mobility Ge channel integration in PMOSFET"IEEE 2013.

[8] KhairulAffendiRosli et.al., "A Comparative Study on SOI MOSFETs for Low Power Applications", Research Journal of Applied Sciences, Engineering And echnology 5(8):2586- 2591, 2013 ISSN: 2040-7459; e-ISSN: 2040-7467©Maxwell Scientific Organization, 2013.

[9] Chen et al., "High-performance III-V MOSFET with nanostacked high-k gate dielectric and 3D fin-shaped structure" Nanoscale Research Letters 2012.

[10] Ramanathan et al.,"CMOS-Compatible Vertical-Silicon-Nanowire Gate-All-Around p-Type Tunneling FETs With ≤ 50-mV/decade SubthresholdSwing"IEEE Electron Device Letters, vol. 32, no. 11, November 2011.

[11] Stephen W. Bedell et.al., "Mobility Scaling in Short-Channel Length Strained Ge-on-Insulator P-MOSFETs"IEEE Electron Device Letters, vol. 29, no. 7, July 2008.

[12] Two-Dimensional Analytical Threshold VoltageModel of Nanoscale Fully Depleted SOI MOSFETWith Electrically Induced S/D Extensions.IEEE Transaction on Electron Devices Vol. 52, NO. 7, July 2005.