

A Novel high-speed transistorized 8x8 Multiplier using 4-2 Compressors

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Abstract— In this paper, a novel implementation of 8x8 Multiplier using 4-2 Compressors is presented; which produces quick results, especially for use in Digital Signal Processors and in Microprocessors. This multiplier uses a new partial-product reduction format which consecutively reduces the maximum output delay. The new design of multiplier requires less number of MOSFET's compared to Wallace Tree Multipliers. The 4-2 Compressor used is made from high-speed and low-power XOR-XNOR module and transmission gate based Multiplexer. The delay and power-delay product (PDP) is compared with earlier Wallace and Dadda Multipliers, implemented with 4-2 Compressors and without compressors, and is proven to have minimum delay and PDP. The Simulation results were obtained using HSPICE at 0.18 μ m standard CMOS technology.

Keywords— 4-2 Compressors, partial-product reduction, Reduction format, Tree Multipliers, XOR-XNOR module, Multiplexer, 0.18 μ m CMOS.

INTRODUCTION

With the emerging need for high speed VLSI devices, there is a continuous demand for high speed multipliers, as they are the core elements in several Computer Arithmetic circuit applications like Image Processing, Digital Signal Processors like in Filters, Convolutors; Multimedia like in Oscillators and Microprocessors like in ALU's. The performance of multipliers helps in determining the processor's speed of running and performance of several DSP algorithms. In most of the VLSI systems, multiplier directly lies in the critical path. So, for these reasons, the designers are now focusing on multipliers of high speed and low power delay product.

There are generally three phases in tree multiplier architecture, which are partial product generation phase, partial product reduction phase and finally the addition phase to obtain the final result. Among these three phases, the second phase - partial product reduction phase consumes most of the power and is responsible for overall critical path delay. Therefore in order to optimize this stage, Compressors can be used for partial product accumulation [1]. Compressors are used for addition operation and they contribute for reduced critical path delay, which is important in maintaining circuit's performance [2]. This can be accomplished with usage of 3-2 Compressors (Full-Adders) and 4-2 Compressors. These compressors are internally made of XOR-XNOR and multiplexer modules and their improved design will contribute a lot towards the overall system performance.

In present work, 4-2 Compressor made from high-speed and low-power XOR-XNOR module and transmission gate based Multiplexer was used. A new technique of partial-product reduction using 4-2 Compressors in multipliers have been proposed based on pre-determined sequence of matrix heights to give minimum number of partial-product reduction stages, with reduces delay and PDP of multiplier and has lesser transistor count.

This paper is organized as follows: In section 2, composition of 4-2 Compressor and its design is described. In section 3, tree multipliers are discussed and compared. In section 4, Wallace scheme based on compressors is presented and our reduction scheme is introduced. Experimental results and evaluation of our scheme against 4-2 compressor based Wallace schemes are presented in section 5. Finally, we conclude this work in Section 6.

COMPRESSORS

Compressors of type 3-2 and 4-2 are generally used for performing additions. In multiplier design, 4-2 Compressor is ideal for constructing regularly structured Wallace tree with less complexity. Usage of compressors will help to have fewer interconnections. Compressors of higher order can be designed by interconnecting lower order compressors, like a 4-2 compressor can be made from two full adders.

A. Composition of Compressors

Compressors are composed of XOR - XNOR gates and Multiplexers. There are several different XOR-XNOR and Multiplexer modules reported in literature. XOR-XNOR gates are also used as building blocks in Parity Checkers, Oscillators, and Comparators etc. Static CMOS based XOR-XNOR uses both pMOS and nMOS consumes many transistors and larger area [3]. Static XNOR-XOR also uses Complementary CMOS style but they both consume large power and not used at low voltages [4]. The XOR-XNOR with feedback transistors can be used at low voltages but input load is doubled, causes slow response if cascaded [5] and area increased. XOR-XNOR shown in Figure 1 uses only 8 transistors and can operate well at low supply voltages. It also provides good driving capability and has high speed performance than the prevailing three XOR-XNOR gates [1].

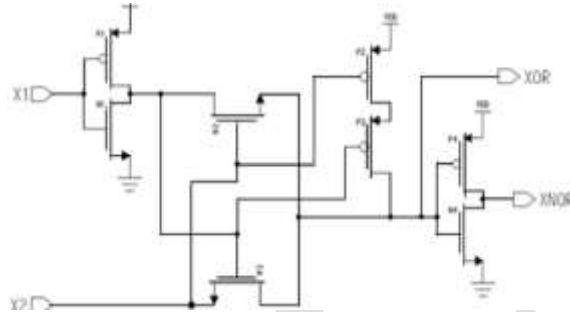


Figure 1: Circuit diagram of XOR-XNOR for good driving capability, low area

Multiplexer (MUX) module is used for Carry generation in Compressors. MUX output is based on Select lines (S). If there are 2 data inputs, it is called 2-1 MUX. Static MUX [3] and MUX with transmission gates and output buffer consume larger area and delay. So, MUX with transmission gates shown in Figure 2 can be used in Compressors for use in low power cells for faster results within low area consuming 6 transistors [6].

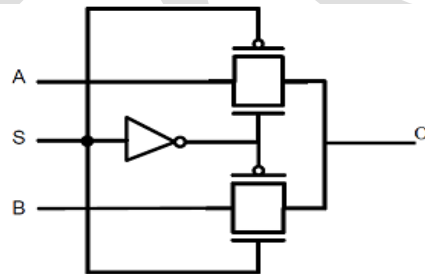


Figure 2: MUX with transmission gates

B. Design of a 4-2 Compressor

Mostly 3-2, 4-2 Compressors are generally used. A 3-2 Compressor is also called a Full Adder Cell [7] with 3 equal weighted inputs and Sum, Carry outputs. 4-2 Compressor can be built from 2 Full-Adders connected serially. It has 5 inputs called X1, X2, X3, X4 and Cin and produces 3 outputs Sum, Carry and Cout, where Carry and Cout have one bit higher weight than others. Here the Cin and Cout are independent to each other [8]. The Block diagram, logical decomposition of 4-2 compressor is shown in Figure 3,

On using the above mentioned XOR-XNOR and MUX modules, the 4-2 Compressor requires fewer transistors (only 40 transistors), and so low area and also the power consumption is minimal. The resulting output's delay is also minimized when MUX block is used at Sum output instead of XOR-XNOR as the select bit is given prior that causes transistor switching before inputs arrive [9]. The equations governing outputs are,

$$\begin{aligned} \text{Sum} &= (X1 \oplus X2) \cdot \overline{X3 \oplus X4} + \overline{(X1 \oplus X2)} \cdot (X3 \oplus X4) \cdot \overline{\text{Cin}} + \overline{(X1 \oplus X2)} \cdot \overline{X3 \oplus X4} + (X1 \oplus X2) \cdot (X3 \oplus X4) \cdot \text{Cin} \\ \text{Carry} &= (X1 \oplus X2 \oplus X3 \oplus X4) \cdot \text{Cin} + \overline{(X1 \oplus X2 \oplus X3 \oplus X4)} \cdot X4 \\ \text{Cout} &= (X1 \oplus X2) \cdot X3 + \overline{(X1 \oplus X2)} \cdot X1 \end{aligned}$$

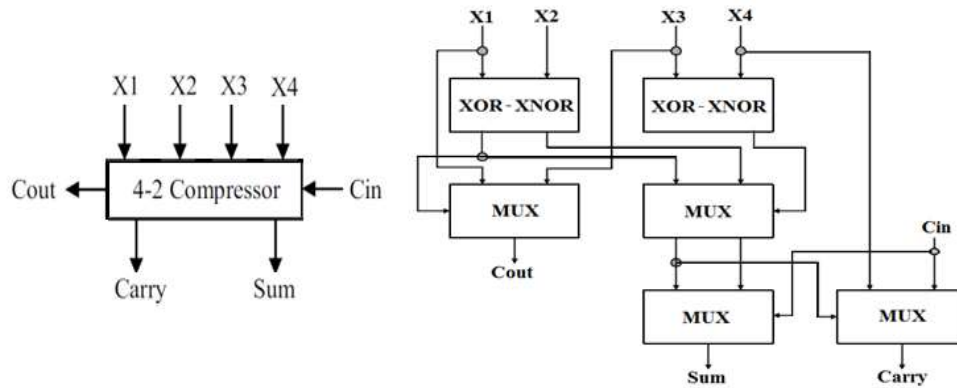


Figure 3: Block diagram, Logic Decomposition of 4-2 Compressor

The critical path delay of the above mentioned 4-2 compressor is one XOR and two MUX delays.

BASIC TREE MULTIPLIERS

The Tree (parallel) multipliers are generally highly performance efficient. In these tree multipliers, first phase of partial product generation is implemented by multiplying each multiplicand bit with the multiplier bit by AND operation. The Tree multipliers like Wallace and Dadda differ mainly in the Partial product reduction phase based on the type of reduction algorithm used. The last addition phase performs addition of the reduced bits using Carry Propagate Adder (CPA) to produce the final result.

A. Wallace Tree Multiplier

Wallace Tree multiplier accumulates partial products column-wise into three and two bits and gives them to Full-Adders and Half Adders respectively to reduce as Sum, Carry bits. Any bit that does not belong to these adders are bypassed to next stage and carry is propagated to one-bit higher order column of next stage. Wallace accumulates as many bits as possible into adders [10]. At each stage, this process is continued until the stage height is reduced to 2 rows. The Wallace tree 8x8 multiplier along with its reduction stage is shown in figure 4, with five stages. Stage 5 uses Carry Propagate Adder. A total of 47 Full-adders and 17 Half-adders are used for Wallace 8x8 multiplier.



Figure 4: 8x8 Wallace Tree Multiplier

B. Dadda Tree Multiplier

Dadda proposed an algorithm with predetermined sequence of matrix (stage) heights for $N \times N$ multipliers to have reduced number of reduction stages. It is developed by working back from two row stage. The height of each intermediate stage is limited to floor value of 1.5 times the height of the successor stage [11].
 i.e., Height of stage $i = (3/2) * \text{Height of stage } i+1$. Then sequence of stage heights are 2,3,4,6,9,13...



Figure 5: 8x8 Dadda Tree Multiplier

The 8x8 Dadda tree multiplier at 5 stages is shown in Figure 5. The recursive algorithm used in partial product reduction of a Dadda Multiplier (here 8x8) is as follows,

The maximum height of an 8x8 multiplier is 8 bits. The next stage height should be 6, so after reduction, the maximum column (C) size should be 6.

Step 1: C1 – C6 have column height less than or equal to 6. So, no need to change these columns.

Step 2: C7 has 7 bits. So, to reduce it into 6 bits, a half adder has to be used.

Step 3: C8 has 8 bits and a carry from C7. So, to reduce 9 bits to 6 bits, a half and full adder is required.

Step 4: C9 has 7 bits and two carry bits from C8. So, a half and full adder are needed to reduce to 6 bits.

Step 5: C10 has 6 bits and two carry bits from C9. So, to reduce these 8 bits into 6, a full adder is required.

After these steps, there will be 6 bits or less than 6 bits in every column from C11 onwards. From stage height formula, the next stage heights are to be 4, 3, 2. So, by following above reduction steps, the maximum column (C) sizes are maintained as 4, 3, 2 respectively by appropriately using full adders, half adders wherever necessary. The number of full and half adders needed in Dadda reduction are N^2-4N+3 and $N-1$ respectively for an $N \times N$ multiplier. Then the resulting 2 rows are given to adder stage. Totally, 48 Full-adders and 8 Half-adders are used for Dadda 8x8 multiplier including the reduction and addition stage.

The main difference between Wallace and Dadda multipliers is that, Wallace uses adders wherever possible but Dadda uses adders wherever necessary in order to maintain the predetermined stage height. The critical path is varied and so, delay of Dadda is less than that of Wallace as Dadda is intended to save number of adders. The delay and power delay product (PDP) comparison of Wallace and Dadda 6X6 and 8X8 multipliers are shown in table 1.

Table 1: Delay and PDP Comparison in Wallace and Dadda Multipliers

Type of Multiplier	NxN	Delay (nS)	PDP (10^{-14} J)
Wallace	6x6	4.724	73.17
Dadda		1.907	31.83
Wallace	8x8	11.47	512
Dadda		9.242	371.8

MULTIPLIERS BUILT FROM 4-2 COMPRESSORS

Compressors when used in partial product reduction phase in multipliers will help in having lesser number of interconnections and adder cells. As 4-2 compressor has less delay compared to two full adders; in high speed multipliers, using compressors instead of conventional adders lead to fast output generation and also the number of reduction stages gets reduced. The 4-2 compressor shown in Figure 3 is better suitable in Multiplier's design as it requires lesser transistor count and it provides better performance.

A. Wallace Tree Multiplier using 4-2 Compressors

8x8 Wallace Multiplier using 4-2 compressors (rounded rectangles) is shown in Figure 6. On using compressors the number of reduction stages gets reduced to 3, instead of 5 stages when only half and full adders are used. The delay and thus PDP also gets reduced [12]. The Multiplier uses 17 no. of 4-2 Compressors, 18 full adders and 9 half adders. This Wallace tree has lesser delay compared to the one which does not use 4-2 compressors.

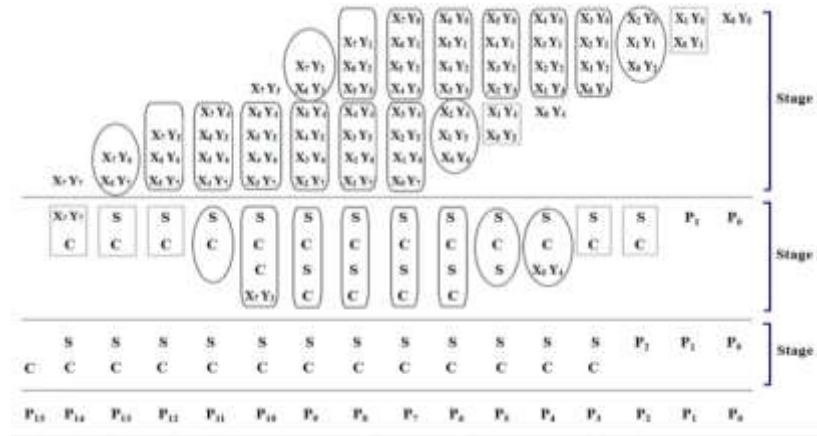


Figure 6: 8x8 Wallace Tree Multiplier using 4-2 Compressors

B. Proposed 8x8 Multiplier using 4-2 Compressors

For NxN multipliers, we introduce a partial product reduction format which is having predetermined stage heights for having high speed multiplications. After the partial product generation stage, the maximum stage height (of stage 1) is N for NxN multipliers. In our scheme,

Height of subsequent stages = $2^{(m-i)}$, where 2^m is nearest smaller integer to N; i ranges from 0 to m-1.

The stage heights are Stage 2 = 2^m , Stage 3 = 2^{m-1} , Stage 4 = 2^{m-2} ... until final stage height is 2. This format is performed with usage of 4-2 compressors (in Figure 3) while maintaining stage height. The 8x8 multiplier with the proposed scheme is shown in Figure 7. The maximum height of partial products stage (Stage 1) is 8 bits. The nearest 2^m integer smaller than $8(2^3)$ is 4 i.e., $2^{(2-0)}$. So, the height of Stage 2 should be 4 bits, which is maximum column (C) height. Examine each column (C) and the reduction is as follows,

- Step 1: C1 to C4 have height less than or equal to 4 bits. So, no need to change these columns.
- Step 2: C5 has 5 bits and to reduce it to 4 bits, a half adder is required.
- Step 3: C6 has 6 bits and a carry bit from C5. A 4-2 Compressor is required to make its height 4 bits.
- Step 4: C7 has 7 bits and a carry from C6. A 4-2 Compressor and half adder are needed to reduce it to 4 bits.
- Step 5: C8 has 8 bits and 2 carry bits from C7, and so two 4-2 Compressors are required.
- Step 6: C9 has 7 bits and 2 carry bits from C8. So, two 4-2 Compressors are needed with one of its input as 0.
- Step 7: C10 has 6 bits, 2 carries and Cout from C9. A 4-2 compressor and full adder are needed to reduce it to 4 bits.
- Step 8: C11 has 5 bits and 2 carries from C10. So, one 4-2 compressor is required.
- Step 9: C12 has 4 bits and a carry, Cout from C11. So, a full adder is required, after which each column has less than or equal to 4 bits.



Figure 7: Proposed 8x8 multiplier using 4-2 Compressors

Next stage height is to be $2^{2-1} = 2$ which is last stage. The reduction steps to have maximum column height 2 are

Step 1: C1, C2 needs no changes in them, but C3 has 3 bits. So, a half adder is required to reduce to 2 bits.
 Step 2: C4 has 4 bits and carry from C3. Thus, a 4-2 compressor is needed
 Step 3: C5 to C13 has 5 bits including a carry from just preceding columns. So, a 4-2 compressor is required.
 Step 4: C14 has 2 bits and a carry, Cout from C13. So, a full adder is required to reduce it 2 bits.

Now, after this stage each column has less than or equal to 2 bits, after which the reduction phase is completed and this last stage is given to Carry Propagate Adder for producing the final multiplier result. This proposed 8x8 multiplier uses 18 no. of 4-2 Compressors, 16 full adders and 4 half adders.

This proposed reduction format using 4-2 Compressors can be applied to any NxN multiplier of N (≥ 4) to have high speed and lesser transistor count even than that of Wallace Tree multiplier using 4-2 Compressors. For example 10x10, 12x12, 16x16 multipliers, all will have the next stage heights as 8, 4, 2 bits.

EVALUATION AND EXPERIMENTAL RESULTS

With the proposed reduction format usage in multipliers, the reduction stages gets reduced and also the output delay and further power delay product (PDP) gets reduced as 4-2 Compressors have less delay and number of interconnections than multipliers with full adder cells. This present format provides even better speed performance than Wallace tree Multiplier which uses 4-2 Compressors (as in Figure 6) and also utilizes lesser number of transistors. This can be noticed from the comparison Table 2 between Wallace multiplier using 4-2 Compressors and Proposed Multiplier format. The Inputs(X, Y) and Simulation results ($P_0 - P_{15}$) of the proposed 8x8 multiplier using 4-2 Compressors is shown in Figure 8(A) and 8(B) with a supply voltage of 3.3V.

Table 2: Comparison of Proposed Multiplier Format against Wallace using 4-2 Compressors

Type of Multiplier	NxN	Number of transistors	Delay (nS)	PDP (10^{-14} J)
Wallace	6x6	852	4.030	61.48
Proposed		792	1.348	22.81
Wallace	8x8	1532	10.94	497.9
Proposed		1472	6.749	359.57



Figure 8(A) Inputs X, Y of Proposed 8x8 multiplier

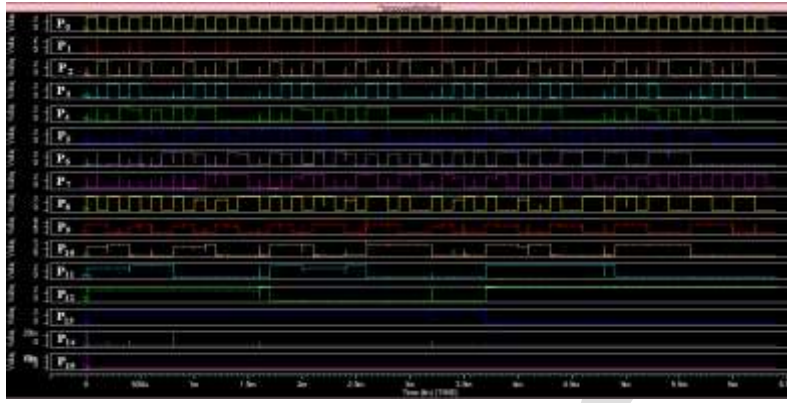


Figure 8(B) Simulation results ($P_0 - P_{15}$) of the proposed 8x8 multiplier

CONCLUSION

A novel transistorized 8x8 multiplier has been presented for high speed performance, which uses 4-2 compressors based on an XOR-XNOR gate of high speed and low power and Multiplexer made of transmission gates. This proposed multiplier uses a reduction format with predetermined stage heights for having quick results and further minimum power delay product (PDP). When the Simulation results were performed using HSPICE at 0.18 μ m CMOS technology, the 8x8 multiplier shows optimal speed performance against basic Dadda Tree multiplier and Wallace Tree Multiplier implemented with and without 4-2 Compressors with minimal transistor count and PDP. This proposed reduction format can also be applied to higher order NxN multipliers for high speed results.

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