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A SURVEY ON HIGH SPEED CONVOLUTION AND DECONVOLUTION SYSTEM BASED ON FPGA

Miss.Priya R.Jain [1]

[1]PG Student of HVPM'S College of Engineering and Technology Amravati (India)

Email: priya_20jain@rediffmail.com

Contact No- +917304790304

Prof. Dr.Ujwalla A.Bellorkar [2]

[2]Head & Asst. Professor in Dept. of HVPM'S College of Engineering and Technology Amravati (India)

Abstract— In Digital Signal Processing, the convolution and deconvolution with a very long sequence is ubiquitous in many application areas. They consume much of time. This paper presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The most significant aspect, is the development of a multiplier and divider architecture based on high speed algorithm. It shows that the implementation of linear convolution and circular convolution is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures. In this paper we study different forms of high speed convolution and deconvolution system using FPGA.

Keywords— Linear *Convolution*, Circular *Convolution*, Deconvolution, Radix-2 Booth Multiplier, Radix-4 Booth Multiplier**,** Vedic Mathematics, Urdhav Tiryagbhyam, Digital signal processing, ,VHDL.

INTRODUCTION

Convolution and deconvolution is the most important and fundamental concept in signal processing and analysis. However, beginners often struggle with convolution and decovolution because the concept and computation requires a number of steps that are tedious and slow to perform. Therefore many of researchers have been trying to improve performance parameters of convolution and deconvolution system using new algorithms and hardware. Complexity and excess time consumption are always the major concern of engineers which motivates them to focus on more advance and simpler techniques. Pierre and John have implemented a fast method for computing linear convolution, circular convolution and deconvolution . This method is similar to the multiplication of two decimal numbers and this similarity makes this method easy to learn and quick to compute. Also to compute deconvolution of two finite length sequences, a novel method is used. This method is similar to computing long-hand division and polynomial division .Following diagram shows the overall process of high speed convolution and deconvolution process.

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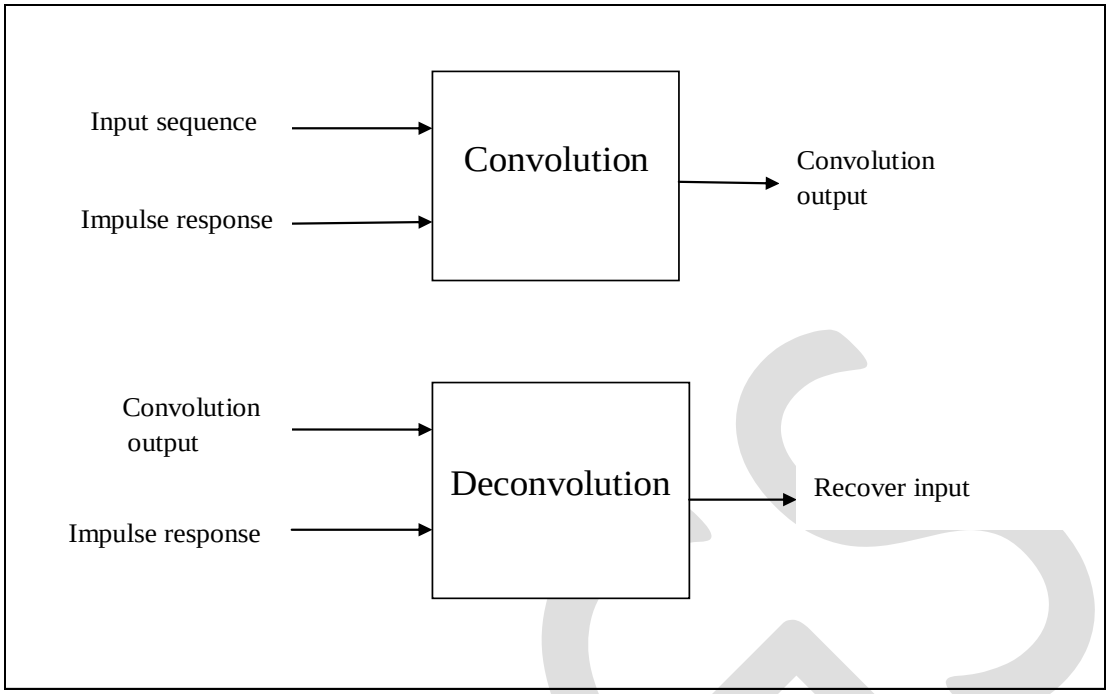

Fig . Block diagram of Convolution and Deconvolution system

With the latest advancement of VLSI technology, digital signal processing plays a pivotal role in many areas of electrical engineering. Discrete convolution is central to many applications of Digital Signal Processing and Image Processing. It is used for designing of digital filter and correlation application. However, beginners often struggle with convolution because the concept and computation requires a number of steps that are tedious and slow to perform. The most commonly taught approach is a graphical method because of the visual insight into the convolution mechanism. Graphical convolution is very systematic to compute but is also very tedious and time consuming. The principal components required for implementation of convolution calculation are adder and multiplier for partial multiplication. Therefore the partial multiplication and addition are bottleneck in deciding the overall speed of the convolution implementation technique. Complexity and excess time consumption are always the major concern of engineers which motivates them to focus on more advance and simpler techniques.

LITERATURE REVIEW :

Surabhi Jain & Sandeep Saini [1] presents a direct method of computing the discrete linear convolution, circular convolution and deconvolution. The approach is easy to learn because of the similarities to computing the multiplication of two numbers. The most significant aspect of the proposed method is the development of a multiplier and divider architecture based on Ancient Indian Vedic Mathematics sutras Urdhvatriyagbhyam and Nikhilam algorithm. The results show that the implementation of linear convolution and circular convolution using vedic mathematics is efficient in terms of area and speed compared to their implementation using conventional multiplier & divider architectures.

G.Ramanjaneya Reddy, A. Srinivasulu [2] presents an on the spot methodology of reducing convolution processing time using hardware computing and implementations of discrete linear convolution of two finite length sequences (NXN). This implementation method isrealized by simplifying the convolution building blocks. The purpose of this analysis is to prove the feasibility of an FPGAthat performs a convolution on an acquired image in real time. . In addition, the presented circuit uses less power consumption and delay from input to output. It additionally provides the required modularity, expandability, and regularity to form different convolutions for any variety of bits.-+.

Sukhmeet Kaur, Suman and Manpreet Signh Manna [3] describes implementation of radix-4 Modified Booth Multiplier and this implementation is compared with Radix-2 Booth Multiplier. Modified Booth's algorithm employs both addition and subtraction and also treats positive and negative operands uniformly .No special actions are required for negative numbers. The Speed and Circuit Complexity is compared, Radix-4 Booth Multiplier is giving higher speed as compared to Radix-2 Booth Multiplier and Circuit Complexity is also less as compared to it.

Madhura Tilak [4] presents a novel method of implementing linear convolution of two proposed method uses modified design approach by replacing the conventional multiplier by Vedic multiplier internally in the implementations. The proposed method is efficient in terms of computational speed, hardware resources and area significantly. The efficiency of the proposed algorithm is tested by simulations and comparisons with different design approaches.The proposed circuit is also modular, expandable and regular which provides flexibility.

Asmita Haveliya [5] describes a block convolution process which is proposed using a multiplier architecture based on vertical and crosswise algorithm of Ancient Indian Vedic Mathematics and embedding it in OLA method for reducing calculations. Found on embedding Vedic multiplication for OLA, there is a considerable improvement in their performance Overlap-Add method (OLA) and Overlap-Save method (OLS) methods are employed.

Rashmi . Lomte [6] describes a methof of two finite length sequences (NXM), is implemented using direct method to reduce deconvolution processing time.The perfomance of the circuit has a delay of 79.595 ns from input to output using 90nm process.The outcome of research is high speed deconvolver implementation is achieved. Since 4×4 bitmultiplier is need of this project, different 4×4 bit multipliersare studied and Urdhava Triyakbhyam algorithm which gives lowest delay among remaining all multipliers is used .

Honey Durga Tiwari, Ganzorig Gankhuyag ,Chan Mo Kim, Yong Beom Cho [7] describes New multiplier and square architecture is proposed based on algorithm of ancient Indian Vedic Mathematics, for low power and high speed applications. It is based on generating all partialproducts and their sums in one step. The design implementationon ALTERA Cyclone –II FPGA shows that the proposed Vedic multiplier and square are faster than array multiplier and Booth multiplier.

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CONCLUSION

The main focus of this paper is to introduce a method for calculating the linear convolution, circular convolution and deconvolution with the help of vedic algorithms that is easy to learn and perform. An extension of the proposed linear convolution approach to circular convolution using vedic multiplier is also introduced which has less delay and area than the conventional method. This paper also introduced a straightforward approach to performing the deconvolution . The Vedic Methods enable the practitioner improve mental abilities to solve difficult problems with high speed and accuracy. Radix-4 Booth Multiplier is giving higher speed as compared to Radix-2 Booth Multiplier and Circuit Complexity is also less as compared to it.

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