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A SURVEY ON DESIGN OF EFFICIENT NONVOLATILE SRAM CELL FOR INSTANT ON-OFF OPERATION

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Abstract— In todays technological world of nanoscale CMOS IC, energy is consumed more and is getting serious problem. To minimize this energy consumption, low voltage circuits are needed. Static random access memory (SRAM) is a key element in wide variety of applications and so considering the need of SRAM cell, NVSRAM have been proposed. NVSRAM provide fast power on-off speeds and imformation doesn't loss even if the power supply is turned off. This paper provide new approach towards designing and modeling of NVSRAM cell using volatile SRAM core. The nonvolatile characteristic and the nanoscale geometry of NVSRAM increases the packing density with CMOS processing technology provides new approaches towards power management, without loss of stored imformation, Hence has potential for major saving in power dissipiation. Also NVSRAM cell has scope for speed improvement as the technology matures.

Keywords— Memory, Volatile memory, Nonvolatile memory, Random access memory(RAM), Static random access memory(SRAM), Non volatile static random access memory(NVSRAM), CMOS IC.

INTRODUCTION

The research for new model that will attain processing speed in terms of exa flop and then into zeta flop order is a major challenge for both system architects and circuit designers. Also there is need for realizations of new components and related circuits that are compatible with CMOS processing technology as CMOS scaling begins to slow down. This need for the realization of new circuits has arise because of the evolutionary growth of networks. In recent technology NVSRAM cell is in more focus and is creating more possibilities towards realization of innovative circuits. In this project we propose and modelled the architecture of NVSRAM cell for instant on-off operation using 45nm VLSI/CMOS technology. A typical SRAM cell consist of 6 transistors. SRAM cell is used with non volatile memory and can be fabricated as an extention to CMOS processing technology and addressing the current research towards reduction of power utilization.

Conventional SRAM cell

To appreciate some of the benefits of the proposed architecture we provide brief overview of conventional SRAM cell. The 6T SRAM cell has 2 back to back connection of inverters using N1,P1,N2, P2 and has 2 access transistors. The inverters are used to store either single bit '0' or '1'.Also 'WL' is used to turn on the access transistors and BL,/BL are bit lines through which bits are apply. SRAM cell has three different states it can be in standby where the circuit is idle, reading when data has been requested and writing when updating the contents [4].However one of the known problem for conventional 6T SRAM cell for ultra low power applications is its static noise margin.SNM is an important factor in consideration of write and read operation. Sunil jadav has shown that SNM is reduced by using adiabatic technique [3]. However inclusion of nonvolatile memory in the architecture ensures that data is retained even if the power supply is removed and enabling new possibility in the system design by including all of the important issue of power management.

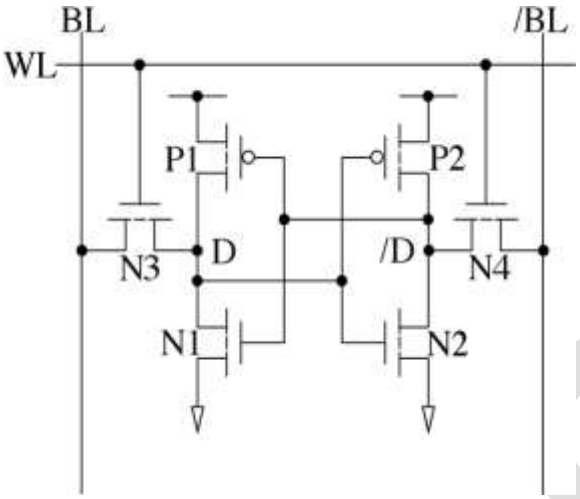

Fig.1.Conventional 6T SRAM cell

LITERATURE REVIEW AND RELATED WORK

From the review of the related work and available literature it is observed that many researcher have designed NVSRAM cell by applying their own techniques. NVSRAM is one of the advanced NVRAM technology which is fast replacing the battery backed SRAMs which need battery free solutions. The proposed NVSRAM cell is to be designed using CMOS/VLSI technology. Wei wei has researched on design of 7T1R SRAM cell for instant on operation. This proposed cell provides better nonvolatile performance such as power down, restore and store operation[1].Pankaj kumar pal has researched on dual k spacers technology to enhance SRAM performance in terms of robustness , access time and leakage power [2].Sunil jadav designed ultra low power 6T SRAM using adiabatic technique and by this technique average power dissipiation and static noise margin is also reduced [3].K. Dhanumjaya designed conventional 6T dynamic 8T SRAM cell and achieved improved read stability, read current and leakage current[4].Keejong kim design a low power SRAM using Bit-line charge recycling method and achieved reduced power dissipiation in write cycle[5].Yi-Bo Liao has researched on design of gate-all-around silicon MOSFETs for 6T SRAMs area efficiency. This research is on area efficiency means architecture is designed in minimum cell area[6]. Mi Chang Chang has researched on transistor and circuit design optimization for low power CMOS.As the power is leaked during read-write cycle hence for power management this research has been taken [8].After reviewing all of these researched paper and considering the demand of today's fast communication world, research has been taken to design low power efficient NVSRAM cell using 45nm CMOS/VLSI technology.

PROPOSED WORK

NVSRAM is more advanced NVRAM technology. It has some advantages over conventional 6T SRAM. In conventional SRAM power get lost if the power supply get disabled however in NVSRAM power doesn't lost even if the power supply get disabled. Thus we proposed the architecture of NVSRAM cell by adding non volatile memory to conventional SRAM and trying to make the architecture more efficient. In these subsections, variations of NVSRAM cells as well as brief architecture description is mentioned .The objective in this project are to design and verify the conventional SRAM cell, to design the NVSARM cell by utilizing volatile SRAM core, to design the SRAM cell for 'instant on' operation, to design the CMOS layout of NVSRAM cell using microwind tool based on 45nm CMOS technology and to analyze the NVSRAM cell for area, power and propogation delay. The NVSRAM cell forms a feedback structure. Due to this feedback structure a low input value on the first inverter will generate high value on second inverter which amplifies and stores the low value on the second inverter. Similarly a high input value on the first inverter will generate a low input value on the second inverter , which feeds back the low input value onto the first inverter. Therefore the 2 inverters will store their current logical value, whatever value that is. Also the stored value doesn't lost even if the power supply get turned off because of

the nonvolatile element used in the structure. Hence the structure efficient nonvolatile SRAM cell is proposed. The general model for non volatile memory with 6T SRAM cell as core is as follows.

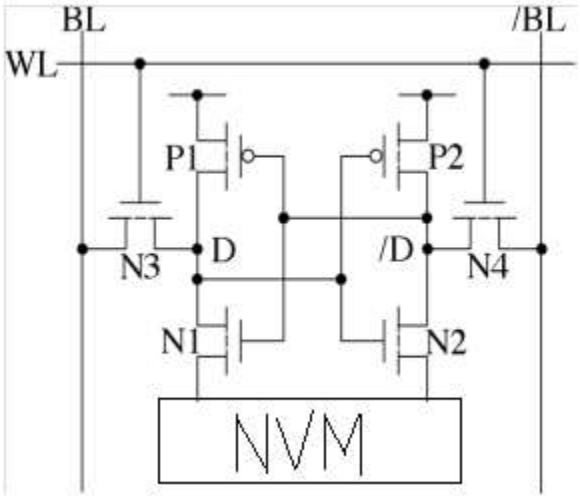

Fig.2.General model for NVSRAM Cell

The proposed NVSRAM cell can be in one of the 3 states as follows. It can be either in

Standby: If the word line is not inserted, the access transistors disconnect the cell from the bit lines. The two cross coupled inverters will continue to reinforce each other as long as they are connected to the supply [4].

Reading: Assume that the content of the memory is a 1, stored at D. The read operation is done by using the sense amplifiers that pull the data and produce the output. The row and column decoders are used to select the appropriate cell or cells from which the data is to be read and are given to the sense amplifiers through transmission gate [4].

Writing: The start of a write cycle begins by applying the value to be written to the bit lines. If we wish to write a 0, we would apply a 0 to the bit lines, i.e. setting BL bar to 1 and BL to 0. A 1 is written by inverting the values of the bit lines. WL is then inserted and the value that is to be stored is latched in. The reason this works is that the bit line input-drivers are designed to be much stronger than the relatively weak transistors in the cell itself, so that they can easily override the previous state of the cross-coupled inverters [4].By reducing the number of components i.e. cmos transistor while designing should be less. Also software tool used in this project for the implementation of efficient non volatile SRAM cell is "microwind". Thus we proposed efficient NVSRAM cell and will try to make it more efficient

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CONCLUSION

NVSRAM are applicable in area such as Medical equipment, in commercial vehicles, in case of external power failure also applications in environments where field service is not possible/costly . A complete functional analysis is given to explain how the proposed cell operates with respect to timing, variation and stability. Considering the advancement of future technology and advantage of 45nm technology the future project has been decided to do with selection of higher order of nm technology. Thus considering all of the details about the demand of today's fast communication world, the research has been taken to design efficient non volatile SRAM cell for instant on-off operation using 45nm CMOS/VLSI technology.

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