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IMPLEMENTATION OF MIMO-OFDM TRANSCEIVER ARCHITECTURE DESIGN WITH SIMULINK

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Abstract— In modern world of communication systems, various new methods have developed to replace the previous conventional techniques that provide data communication with high speed. As wireless communication guidelines were developed it became necessary to develop new techniques like Orthogonal Frequency Division Multiplexing (OFDM) for data security and reliability while data transmission. Idea behind the high spectral efficiency of OFDM is elimination of guard bands and use of the overlapping but orthogonal subcarriers. The communication process to optimize the energy consumption level on the original transmission input signal level and the signal process is to effectively improve the wireless communication applications. This technology is to be modified using the HARDWARE based VLSI architecture. The architecture will improve the transceiver performance in 802.11 MIMO-OFDM systems. This system will be designed the 4*4 MIMO-OFDM architecture in MATLAB-simulink software.

Keywords— MIMO, OFDM, QAM, FFT, IFFT, Intercarrier Interference, MATLAB-simulink**.**

I. INTRODUCTION

The need of high data rate with the bulk of data to be transmitted have led to the improvisation of old and new techniques used for communication. Previous technologies were focused on quality of the signals to be maintained throughout the communication path. On contrary today's scenario focuses on quality as well as high data rate. As wireless communication guidelines were developed, it became the necessity to focus on multi-user supporting technique like OFDM for data security and reliability while data transmission.

OFDM is a special type of multi-carrier transmission technique where a single data stream is transmitted over a number of lower rate subcarriers. In high speed digital communication, the OFDM technique is widely used against frequency selective fading and inter-symbol interference.

MIMO system is the wireless communication system with multiple antennas at the transmitter and receiver has received remarkable attention because of its ability to increase system capacity and performance with acceptable bit error rate (BER) in proportion with the number of antennas. The fusion of MIMO-OFDM is advantageous [1]. Fig.1 shows the generalized block diagram for the OFDM system.

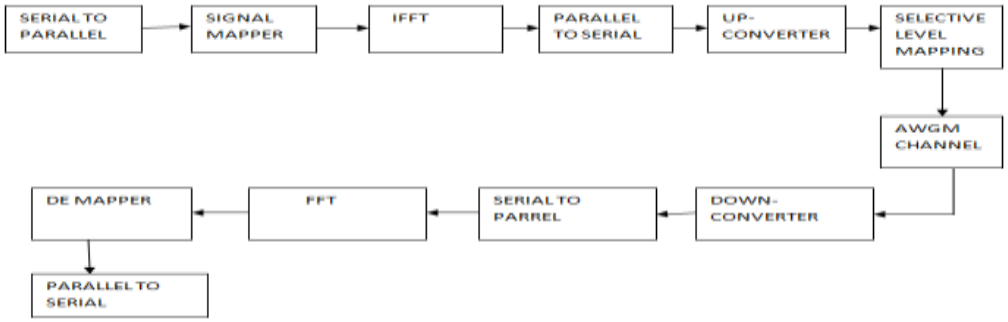

Fig.1 Generalized block diagram for the OFDM system[2]

The use of multiple-input multiple-output (MIMO) signal processing with orthogonal frequency division multiplexing (OFDM) can provide enhanced data rated for the next generation wireless communication systems. But as MIMO-OFDM system transmits multiple data streams, it requires various independent baseband processors. This increases its hardware complexity tremendously when compared with single-input single-output OFDM (SISO OFDM) systems. A very high data throughput rate is provided by the IEEE 802.11n standard based on the MIMO OFDM system.

In proposed system blocks in simulink unit are designed. And to modify the block arrangement in overall OFDM-MIMO unit and to develop the sub system functions also. This process is to optimize the transmission timing about MIMO architecture process. The system generator and Xilinx software are used to implement the hardware architecture about simulink 802.11 MIMO-OFDM system design. Section II presents the work related to reducing the complexity of the MIMO-OFDM system design. Section III presents the proposed model for the 802.11 MIMO-OFDM system design and section IV concludes the paper.

II. RELATED WORK

There are various methods which have been used for designing MIMO OFDM system. A high level Matlab Simulink spatially multiplexed (SM) 4 x 4 MIMO OFDM transceiver encoded at half rate using 64 size FFT was designed and implemented on Spartan Virtex 6 FPGA kit [1]. The simulation, VHDL codes, RTL Schematics and Test Bench for the entire 4 X 4 MIMO OFDM model were obtained to substantiate its functionality.

A spatially multiplexed real time 4 x 4 MIMO OFDM transceiver using 16 QAM was designed and implemented on Spartan Vitex-6 FPGA kit with help of Matlab Simulink, Xilinx and System Generator. A single channel of MIMO transmits four data streams, hence can outbring four times the data rate per channel without extra bandwidth and transmit power. Data rate up to 216 Mbps was accomplished. Each single model were developed and tested using Test benche for its error free functionality and finally all the blocks were collectively mapped. For the implementation of 4 X 4 MIMO OFDM model, the simulation, VHDL codes, RTL Schematics and Test Bench were obtained.

The system designed using VHDL, synthesized using high level synthesis tool and targeted on Xilinx Spartan 3e device. Presented design is simulated on ISE simulator and the results are presented [2]. Resources utilization for transmitter and receiver is given in this paper. The design utilizes the Intellectual Property (IP) cores provided by Xilinx for floating point multiplication, addition, subtraction and division. DIT radix-2 butterfly approach is used to calculate IFFT and FFT.

Idea behind the high spectral efficiency of OFDM is elimination of guard bands and use of the overlapping but orthogonal subcarriers. High rate data stream is divided into a number of low rate data streams that are transmitted over a number of multiplexed orthogonal subcarriers. The low rate data streams allow adding sufficient guard time between two symbols which was very small in high rate data stream. This helps in enabling the system to perform well in dispersive channel which causes the symbols to spread in time and interfere with each other called as inter symbol interference (ISI).

This paper gave the hardware implementation of OFDM system on Spartan 3 FPGA using VHDL language for designing the system. As the number of subcarriers in the system increases, processing time required to calculate IFFT and FFT also increases. The advantage of increasing the subcarrier is the increased spectral efficiency of the system. Device utilization of the transmitter and receiver shows that the device is utilized well below its capacity. Further by increasing the number of subcarriers and by making highly pipelined architecture for IFFT and FFT the system performance could be improved in terms of processing time required in transmitter and receiver.

The custom hardware for MIMO-OFDM system based on FPGA consuming low power was designed [3]. The transmitters and the receivers both were designed for Xilinx Spartan 3E and Spartan 3A FPGA devices. The design was implemented on the FPGA and experiments were performed to substantiate the design. The proposed work [3] proved that a system with very low power can be designed using FPGA device which can provide higher data rate as compared to the ordinary systems and it can be rearranged according to the condition.

This paper study leads to a low power low cost FPGA based reconfigurable architecture which offers effective communication. As it uses the OFDM, it offers faster and huge amount of data transmission without significant interference. It is observed that the data rate is directly proportional to the order of the system. This design is a very simple yet low power consuming and predicted to be an efficient communication chip.

The low power base-band OFDM transmitter and receiver were designed with memory based recursive FFT in FPGA. In the MIMO-OFDM communication system the FFT processor is the most speed calumniatory part. One of the major concerns is low power in this system. The design was implemented by radix-8 FFT and it is observed that the power consumption was decreased by 28% as compared to radix-4 FFT. The architecture [4] had three main pros (a) less number of butterfly iteration to minimize power consumption, (b) pipeline structure of radix-8 butterfly to accelerate clock frequency,(c) even distribution of memory access to utilize efficiency in SRAM ports. The speed performance of the design easily satisfied the requirements of most of the applications and used less number of gates and hence reduced cost and power consumption.

The performance ascertains of four different channel coding and interleaving techniques for MIMO-OFDM communications systems was given. Based on the power dissipation, hardware implementation resources requirement and BER a comparison was done. It [5] presented a low-latency and memory-efficient interleaver implementation method for the MIMO-OFDM communication system. It was the best scheme as far as the power dissipation and hardware resource implication was concerned, which was particularly important

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The implemented systems [5] show a regular improvement in the BER performance and as the constellation size increases there is an increase in the hardware resource utilization, power dissipation, and initial latency. This methodology also provided an effective way to design the IEEE 802.16 system for FPGA. The data rate of the standard was doubled with the help of efficient design methodologies and optimization. Here 64-QAM technique was best among BPSK, QPSK, 16-QAM, and 64-QAM.

The two MIMO-OFDM, E-SDM systems were designed and implemented on hardware of FPGA-based DSP Development Kit. In the systems, orthogonal transmission beams was formed between transmit and receive sides and also optimal transmit input data was adaptively allocated. In addition, a simple detection was used at a receiver to totally eliminate sub-stream interference [6]. The main contribution of this paper was to present the design and implementation of 2x2 and 2x3 MIMO-OFDM ESDM systems on FPGA Altera Stratix DSP Development KIT using Verilog HDL.

Results of BER performance of the systems show that the design is valid and reliable. The comparison of the system performance with that of MIMO-OFDM SDM systems was also performed. Outperformance of MIMO-OFDM E-SDM systems has been shown. The consumption of FPGA elements in the design [6] is also calculated. It is seen that though the E-SDM technique gives a better performance, its hardware consumption is higher than the SDM and STBC techniques due to the complexity of its algorithm.

A design of a variable-length FFT/IFFT processor and its implementation to cover various specifications of OFDM applications is implemented using Verilog HDL in FPGA. The technique of OFDM is famous for its evincing strength against frequency-selective fading channel. The inverse Fast Fourier Transform (IFFT) and FFT operations are used as the demodulation/ modulation in the OFDM systems, and the sizes were varied for FFT/IFFT operations for distinct applications of OFDM systems. The programmable SDF FFT processor can be applied to various OFDM communication systems. This architecture employs a scheme of adding counter to achieve the goal with reduced hardware complexity and also has the advantage of less memory size and lower power consumption [7].

There are various methods which have been used for designing MIMO OFDM system. Idea behind the high spectral efficiency of OFDM is elimination of guard bands and use of the overlapping but orthogonal subcarriers. As the number of subcarriers in the system increases, processing time required to calculate IFFT and FFT also increases which further increases the spectral efficiency of the system. By increasing the number of subcarriers and by making highly pipelined architecture for IFFT and FFT the system performance could be improved in terms of processing time.

III.**PROPOSED MODEL**

The proposed system improves the energy level for the data transmission process in wireless communication system. This system can be used in all type of wireless communication applications. The application mainly focused by the energy consumption level on data transmission unit. The MIMO-OFDM block is to optimize the block and sub system arrangement for proposed system methodology and to reduce the process in the transceiver architecture for the MIMO-OFDM architecture process. This process is to develop the data transmission using MIMO-OFDM 802.11 architecture. The proposed system architecture is design to simulink software and to convert the VHDL code and to implement the hardware VLSI simulation in Xilinx software architecture.

It consists of a serial to parallel/parallel to serial converter, QAM modulator/demodulator and an IFFT/FFT module. The transmitter consists of an input bit stream, serial to parallel converter, constellation mapping, IFFT. The receiver consists of FFT, parallel to serial converter, demodulation, and output bit stream.

A. *Transmitter:*

Data bits are given as a inputs to the transmitter. In order to scatter the input sequence to avoid the dependence of input signals power spectrum on the actual transmitted data these bits passed through the scrambler. Scrambler randomizes the bit sequences. Encoding of data bits can be done with the help of convolution encoder. The mapper is used for mapping and puncturing of data bits; Puncturing removes the some of the parity bits. Different operations of MIMO parser on input data bit are specifically based on spatial multiplexing (SM) and space time block coding (STBC).The protection of data from burst errors during transmission is done by using interleaving. This increases the diversity of wireless system. Pilot insertion plays important role to prevent inter carrier interference. The IFFT block transforms frequency domain signal into time domain signal. Guard interval is introduced to protect orthogonality of subcarriers and the independence of subsequent OFDM symbol.

B. *Receiver:*

The receiver blocks depend on methods used to code the signal in transmitter as it performs exactly opposite operation. The receiver can be divided into three different parts viz. FFT, Synchronization and MIMO detection unit. After receiving the symbol cyclic prefix should be eliminated. Then data is transmitted to the FFT block. FFT block converts time domain signal to frequency domain Receiver is designed separately before connecting it to transmitter. FFT is calculated using an algorithm developed for transmitter. DIT radix-2

butterfly is used to calculate FFT and IFFT. The receiver is designed on Xilinx Project Navigator using VHDL coding. Similar to transmitter, receiver also uses the IP cores for floating point complex multiplication, additions and subtractions. Receiver operations are broken in to different processes and merged to have complete system. After FFT operation, demodulation is done for demodulation look up table approach is used. Once the bits are recovered from the received constellation, the reception is completed. For 4 point and 8 point transmitter separate receivers are designed and tested. Once the design code is ready it is simulated on ISE simulator for timing analysis and then synthesized on kit. Fig 2. shows the design of block diagram in MATLAB simulink.

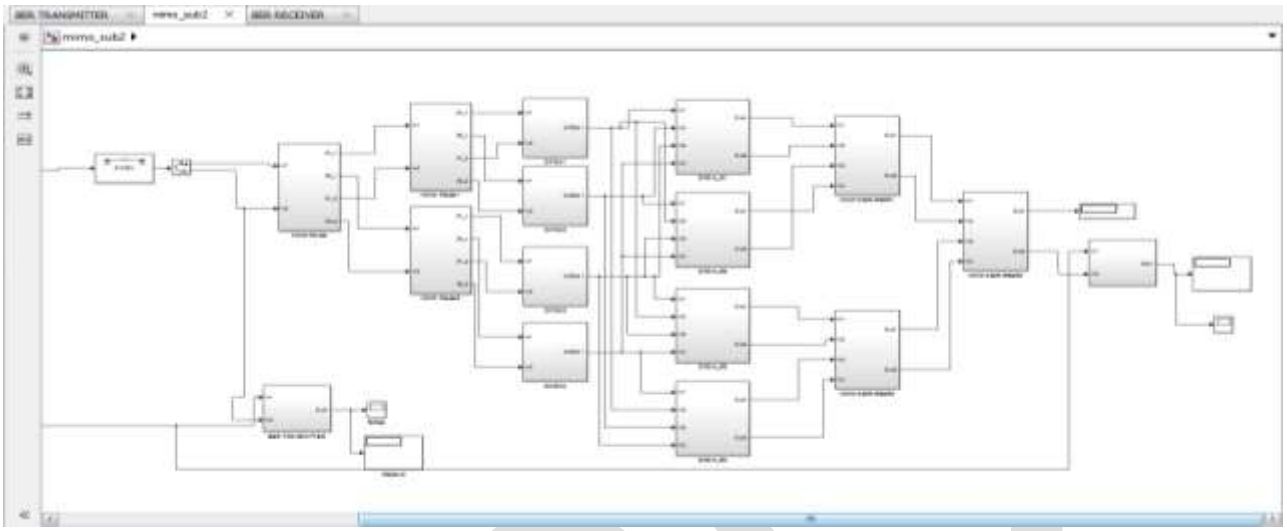

Fig.2 Block Diagram design in MATLAB simulink

IV. SIMULATION RESULTS

The data rate is the ratio of no of data bytes used with the time delay. The data size usage will be 16 K byte. The overall time will be 0.847ns. Data rates up to 1347.2 Mbps are accomplished by transmitting large number of bits/symbol. Thus higher order QAM are required for high data rates. However, as the number of bits per symbol increases, the scheme is more susceptible to the noise and Inter-Symbol Interference. The VHDL codes, RTL Schematics, Test Bench, and power is obtained for the 4 X 4 MIMO OFDM model.

A. *RTL Schematic and Test Bench Generation*

The VHDL codes and its RTL schematics are obtained for the whole model using the ISE Project Navigator. The overall RTL schematics for all the sub models can be viewed inside the main model. With help of ModelSim the test bench simulation is obtained for verifying the correctness of the simulink model. Fig 3 shows the RTL schematic.

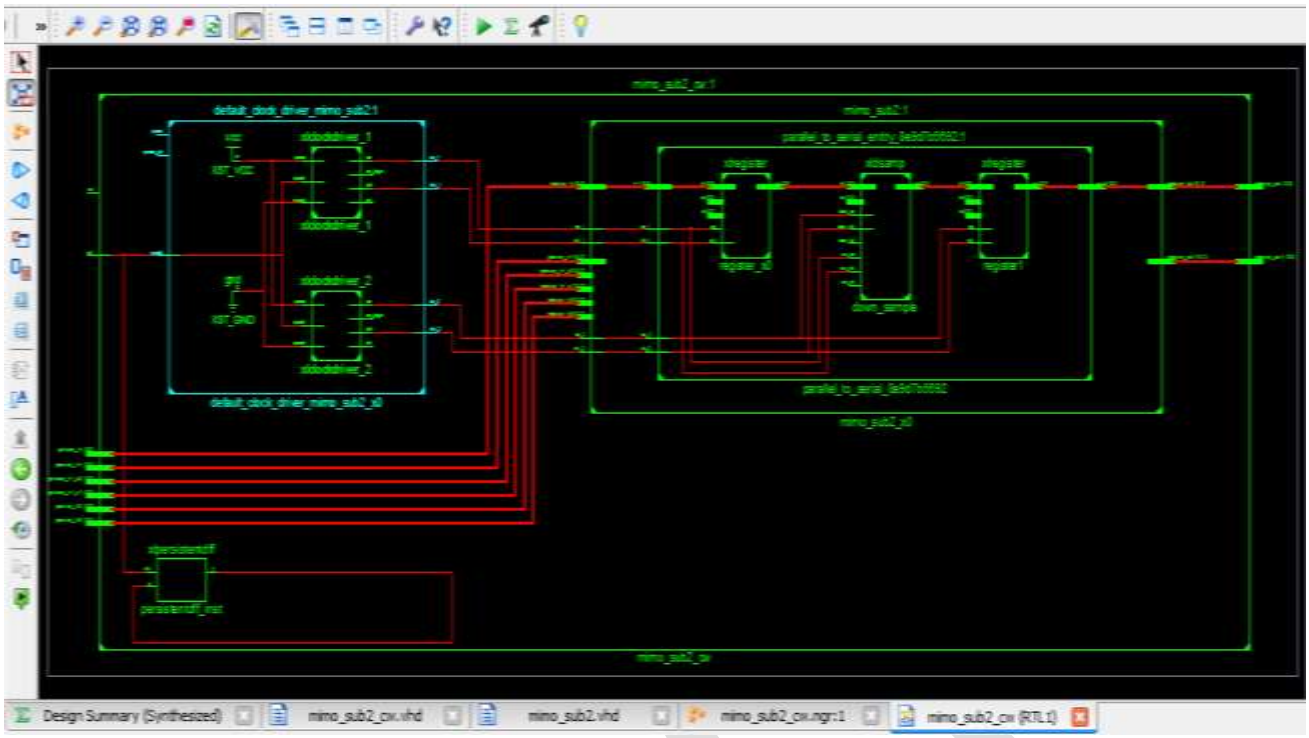

Fig.3 RTL Schematic View

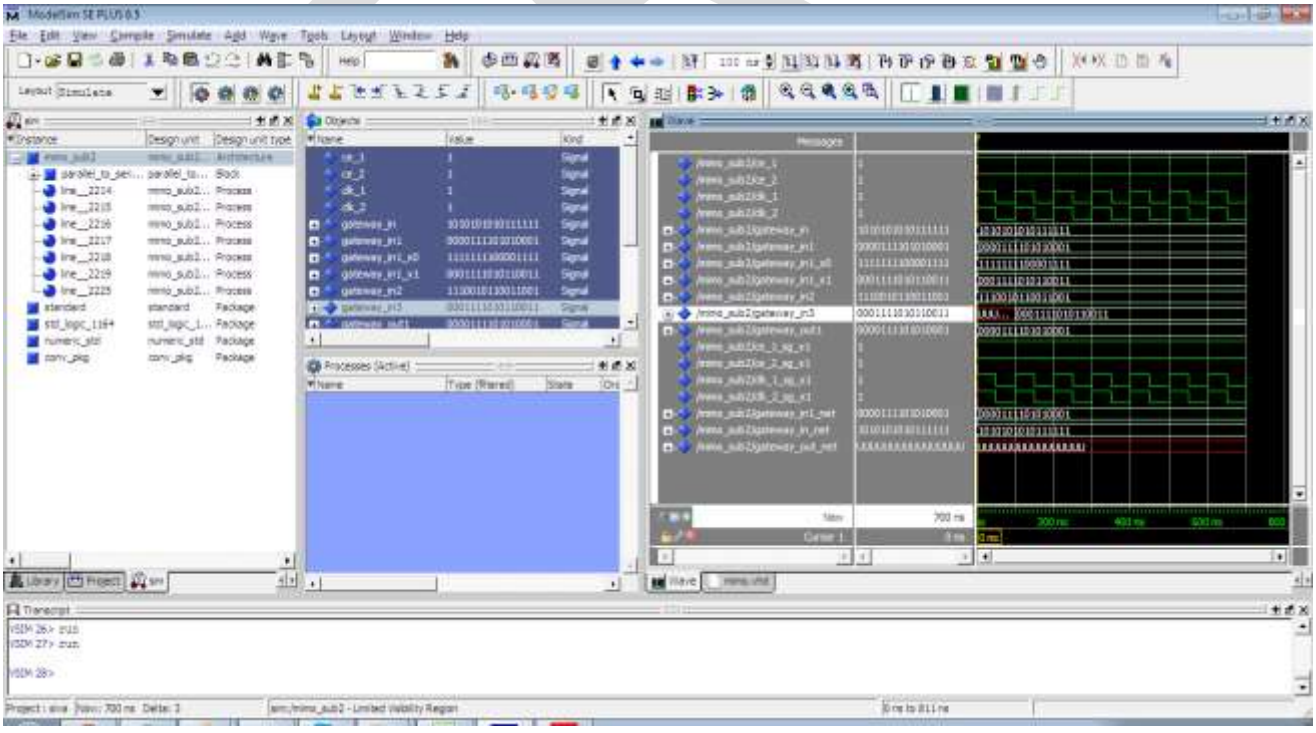

Fig.4 Simulation of 4X4 MIMO-OFDM model in ModelSim

B. *Power Estimation*

The hardware implementation of the design can bring out some important design issues like operating temperature, power consumption, , time delay ,operating frequency that are very important parameters while designing a chip. The design parameter readings taken with the help of Xilinx System Generator are as shown in Table-I.

TABLE I

SIMULINK DESIGN RESULTS

Design issue	Proposed Work
Total dynamic power (in watts)	0.050
Total quiescent power (in watts)	0.085
Total power (in watts)	0.135
Junction temperature (in *c)	30
Maximum frequency (in MHz)	1187.546
Maximum period (in ns)	0.842
No. of IOB used	65
No. of 4 input LUT's used	61
No. of slice flip flop used	60
No. of slices used	60
Data rate(Mbps)	1347.2

V. CONCLUSION

In the design and implementation of OFDM transmitter and receiver, the fusion of MIMO with OFDM results in less BER. The bit error rate with QPSK for OFDM using MATLAB simulation is presented. The BER performance varies and the transmitted bits are received at the receiver section. For this system design on hardware, the MATLAB /SIMULINK software gives visual

modeling tool set that offers the user a library which helps to simulate each hardware components behavior. Then in future work the whole design can be implemented on spartan6 FPGA device. The implementation of this type of design on FPGA is better as compared to ASIC in terms of cost and general purpose MPU in terms of speed. An FPGA means field programmable gate array which supports implementation of relatively large logic circuits.

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