

BOOST PWM CONTROL SCHEME FOR A HALF BRIDGE LLC RESONANT CONVERTER FOR HOLD-UP STATE OPERATION

B.HAREESH¹, N.SRAVANTHI²

PG Student [PE&ED], Dept. of EEE, SISTK, hareesh09212@gmail.com, India¹

Associative professor, Dept. of EEE, SISTK, sravanthin918@gmail.com, Andhra Pradesh, India²

Abstract—In this paper, the proposed converter is predicated on a moiety-bridge LLC resonant converter structure and a single auxiliary switch is integrated at the primary side. The converter has two different operational characteristics. It shows the same operational characteristic with the conventional LLC resonant converters during nominal state. However, when ac line lost and the converter enters into the hold-up time state, which requires wide voltage gain changes, the control method of the proposed converter is transmuted to the PWM method utilizing the auxiliary switch. Since the proposed converter compensates wide voltage gain variation with PWM method of the auxiliary switch, the frequency variation range for the LLC resonant converter is highly reduced in the proposed converter. Therefore the transformer in the proposed converter can be designed at the optimal operating point and it results in decremented conduction loss of the magnetizing inductor current. Furthermore, the maximum voltage gain of the proposed converter is facilely incremented by elongating the obligation ratio of the auxiliary switch. It avails to decrement the link capacitance. To verify the efficacy of the proposed circuit, operational principle will be expounded and experimental results will be presented with following designation. 100 kHz of switching frequency, 250–400 V of input voltage range, 250 V of output voltage, and 75 W output potency.

Index Terms—Boost PWM control and zero voltage switching(ZVS), hold-up time, LLC resonant converter.

1. Introduction

In recent years, considerable researches have been performed for ac/dc converters to increment the puissance density and to amend the efficiency. These researches are mainly fixated on two-stage type ac/dc converter which includes a potency-factor rectification(PFC) stage besides output regulation circuit.

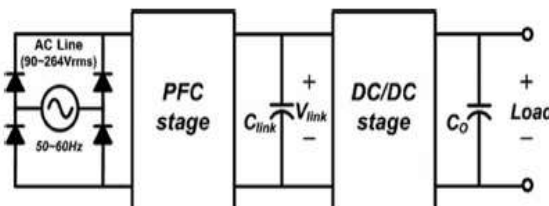


Fig. 1 shows the structure of two-stage ac/dc converter.

The PFC stage is utilized to achieve unity power factor of the system and galvanic isolation and output voltage regulation characteristics are gratified by the dc/dc stage. In these two components, the dc/dc stage is regarded as the more critical part to ameliorate the efficiency of the system, because it converts high voltage input into variable load voltage/current output, which results in a consequential power loss. Furthermore, some designations require that the system.

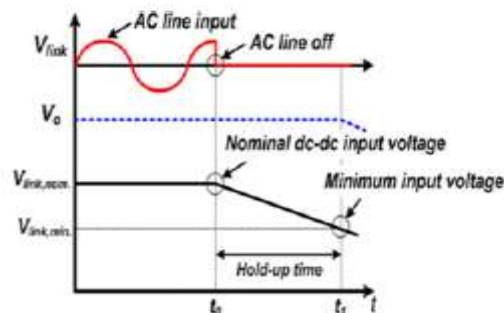


Fig. 2. Input voltage variation of dc/dc converter.

To maintain output voltage for a certain duration after loss of ac line voltage, called hold-up time (visually perceive Fig. 2), which make dc/dc converters have circumscribed efficiency and low power density. The hold-up duration is varied depends on designations, from a few milliseconds to dozens of milliseconds.

During this time, a dc/dc converter is powered by the stored energy in link capacitors, so that the dc/dc converter should be designed to be able to compensate the wide input voltage range. Many approaches have been suggested for a high efficient dc/dc converter [1]–[3]. Among these approaches, LLC resonant converter [3] is culled as the most promising candidate in low power application, due to the zero voltage switching (ZVS) characteristic for the primary switches and no inversion-instantiation quandary for the rectifier diodes. An LLC resonant converter shows the maximum efficiency in the nominal condition, when the converter is operated at the resonant frequency. However, the switching frequency becomes reduced and growing apart from the resonant switching point as the input voltage decreases. This frequency change becomes a considerable issue under a wide input variation condition. It makes LLC resonant converters have arduousness in magnetic design, and it withal decreases nominal efficiency of the converters. The dc conversion ratio of a conventional LLC resonant converter is represented as follows [3]–[5]. A number of different methods have been proposed to surmount this drawback of the LLC resonant converter [5]–[6].

Converter have low power density and incremented circuit intricacy. Boosting-up primary current is another method proposed in Fig.3. The converter applies zero voltage to the transformer utilizing the secondary auxiliary circuit and the primary current is build up during this period. Albeit higher voltage gain characteristic can be achieved with this method, the proposed converter requires many bulk components. Asymmetric PWM control scheme is proposed in Fig.4 [14]. This method increases voltage gain without utilizing any supplemental components, but with transmuted control scheme from frequency modulation(FM) to PWM control for the hold-up time operation. High voltage gain is achieved utilizing this method while maintaining high power density characteristic. However, the gain variation range is constrained in the converter (optically discern Fig3) and the maximum gain is tenacious by the resonant tank design.

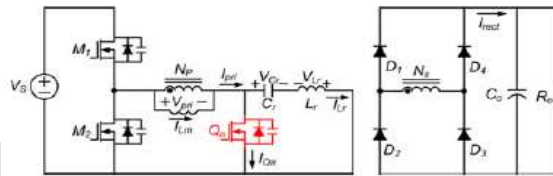


Fig. 3. Schematic diagram of the proposed converter. widely varied in the proposed converter operation, the converter

II. FEATURES OF THE PROPOSED CONVERTER

The circuit diagram of the proposed converter is represented in Fig. 3. It is predicated on the conventional HB LLC resonant converter and an auxiliary switch is integrated to the primary side of the converter. Fig. 8 shows the key operations of the proposed converter for the nominal state and for the hold-up state. In nominal state, the proposed converter is operated just identically tantamount to the conventional LLC resonant converter operated at the resonant switching frequency. The soft switching condition is intuited and no nonessential conduction loss is appeared in this operation. Therefore, the maximum efficiency is showed with the proposed converter during nominal state. When the converter enters into the hold-up state, the converter increases the voltage gain utilizing the auxiliary switch Q_a . The resonant inductor current is build up, while the auxiliary switch is conducted and it is transferred to load during off-state of the auxiliary switch. Therefore, higher voltage gain is easily achieved in the proposed converter by increasing the duty ratio of Q_a . The operational characteristic is similar to the boost PWM operation.

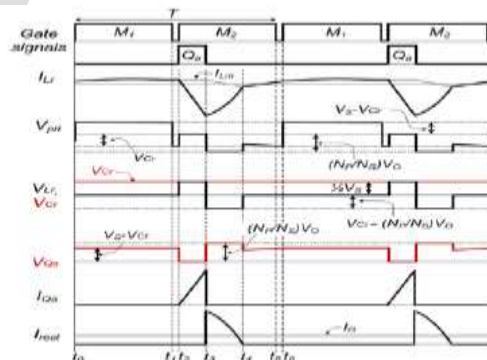


Fig. 4. Key waveforms of the proposed converter.

III. OPERATIONAL PRINCIPLES

Operations of the proposed converter are analyzed in this section. The operational principle for the nominal state is the same with that of the conventional LLC resonant converter operated at resonant frequency [7]–[10]. Thus, only the operation for hold-up time is explained in this section. For the convenience of the mode analysis, several assumptions are made as follows:

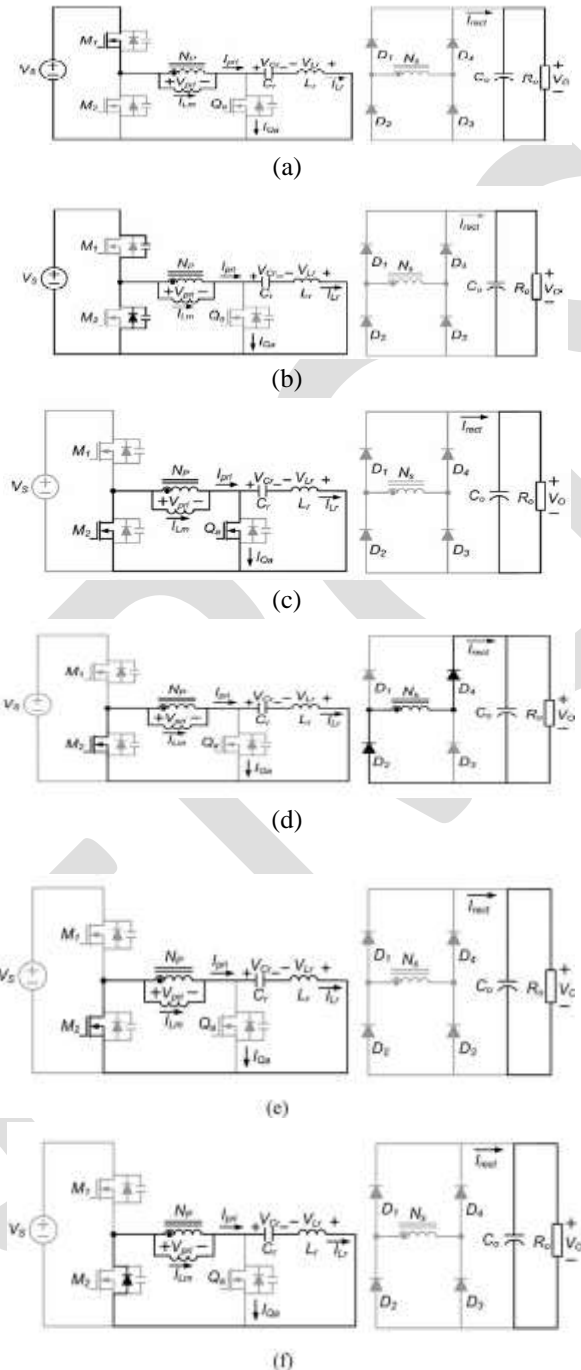


Fig. 5. Equivalent circuit of the proposed converter in hold-up state

A. *Mode 1* ($t_0 - t_1$): The switch M_1 is conducted in this mode and resonant inductor current I_{Lr} resonates with C_r and “ $L_m + L_r$.” The secondary side is disconnected from the primary side and output energy is supplied with the output capacitor.

B. *Mode 2* ($t_1 - t_2$): As M_1 is turned OFF, the parasitic capacitors of M_1 and M_2 start to be charged and discharged, respectively, in a resonant manner. Since the large magnetizing inductor energy is participated in this resonance, ZVS condition of M_2 is easily achieved.

C. *Mode 3* ($t_2 - t_3$): Q_a and M_2 is turned ON at t_2 . HB capacitor voltage V_{Cr} is applied to the resonant inductor L_r and resonant inductor current is linearly increased in this mode. It is expressed as follows:

D. Mode 4 (t_3-t_4): After the Q switch is turned OFF, the built-up resonant inductor current is transferred to the load side. Reflected output voltage is applied to magnetizing inductance of the transformer and negative voltage, " $V_{Cr}-(N_P/N_S)VO$," is found at the resonant inductor L_r . Therefore, the resonant inductor current decreases in this mode.

E. Mode 5 (t_4-t_5): When the resonant inductor current reaches the magnetizing inductor current, I_{Lm} , the secondary side is disconnected from the primary side and resonance between C_r and " L_m+L_r " appears in the converter.

F. Mode 6 (t_5-t_6): M_2 is turned OFF at t_5 and the primary current flows through diode M_2

IV. ANALYSIS AND DESIGN CONSIDERATION

In this section, key characteristics and design considerations of the proposed converter are presented and compared with the conventional LLC resonant converter. Generally, high capacitance design for a resonant capacitor and low inductance design for a resonant inductor are preferred in conventional LLC resonant converters for high power density and high efficiency, so that the capacitor voltage V_{Cr} is regarded as a constant value in this analysis for a more facile understanding of the proposed converter. Also the magnetizing inductor current, I_{Lm} , is considered as a constant value in this analysis during the switching period because the magnetizing inductor L_m is customarily designed to have very high inductance value compared to L_r , so that the current variation of I_{Lm} is neglected in conventional LLC converter operation

A. Voltage on the Resonant Capacitor

The voltage applied to the resonant capacitor V_{Cr} is used to derive the dc conversion ratio and current stress of the proposed converter, and V_{Cr} can be achieved by using the simplified key waveforms. Since each increment of resonant inductor currents Δi_{Lr} during the period of " $D_{Qa}T$ " and " $D_P T$ " are the same, the duration " $D_P T$ " is achieved as follows:

$$\frac{V_{Cr}}{L_r} D_{Qa} T = \frac{(nv_0 - v_{Cr})}{L_r} D_P T$$

$$= \frac{L_r}{(nv_0 - v_{Cr})} D_P T \quad (1)$$

$$0.5T(V_S - V_{Cr}) = nv_0 D_P T + V_{Cr}(0.5 - D_{Qa} - D_P)T$$

(2)

$$V_{Cr} = \frac{0.5v_0 - nv_0 D_P}{1 - D_{Qa} - D_P} = \frac{nv_0 D_P}{D_{Qa} + D_P} \quad (3)$$

Therefore, the resonant capacitor voltage can be represented as (5). It means the half of the input voltage is applied to the resonant capacitor during the hold-up state operation

$$V_{Cr} = 0.5V_S \quad (4)$$

B. DC Conversion Ratio

The proposed converter has two different input-output voltage conversion ratios depending on its operational state. For nominal state, it has the same operational characteristic with the conventional LLC resonant converter. Thus, voltage gain is affected by switching frequency, F_s , and the dc conversion ratio is expressed as

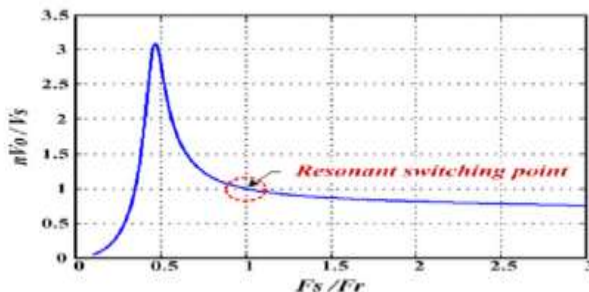


Fig. 6. Dc conversion ratio during nominal period (at 75 W Specification).

At nominal state when the converter has fixed input voltage condition, the proposed converter is operated at the resonant frequency F_r , and the switching frequency is ideally fine-tuned to the resonant frequency at any load condition. The cognition of voltage gain and switching frequency is depicted. A PWM method is adopted in the proposed converter to increment the voltage gain during hold-up state operation. Fig. 8 shows the key wave forms of the proposed converter during hold up state operation. The shaded area AP

implicatively insinuates the total charge Q transferred from the input side to the secondary load side. Thus, output voltage can be derived by calculating the

area of AP , and total charge transferred to the load is represented as follows:

$$Q = 0.5 * \frac{I_{PK} D_{PT}}{T} = \frac{V_o}{R_o} x \frac{1}{n} \quad (5)$$

Since D_{PT} and I_{PK} values in (7) are calculated from the following equations:

$$I_{PK} = \frac{V_{cr}}{L_r} D_{Qa} T \quad (6)$$

$$D_{PT} = \frac{V_{cr}}{(nV_o - V_{cr})} D_{Qa} T \quad (7)$$

The dc conversion ratio of the proposed converter in hold-up operation is expressed as (10) and

As shown in Fig 13, the voltage gain in hold-up state is affected by the duty ratio of Q_a , and the gain is linearly increased followed by the duty ratio.

C. Reduction of the Link Capacitor

After ac line lost, dc/dc converters are powered by energy stored in link capacitors. Therefore, hold-up time condition and the size of link capacitance are the major considerations

$$\frac{1}{2} C_{link} X (v_{nom}^2 - v_{min}^2) \geq p_o t, t = hold - uptime \quad (8)$$

Since the hold-up time condition and output power ratings are given specifications in the system, minimum link voltage is the only one factor which affects the link capacitance design. The equation for the link capacitance design.

$$C_{link} \geq p_o t * \frac{2}{v_{nom}^2 - v_{min}^2} \quad (9)$$

Since the dc conversion ratio of the proposed converter shows linear characteristic, reduction of link capacitor is easily achieved simply by increasing the maximum duty ratio of the auxiliary switch Q_a . Size of capacitors is highly affected by the capacitances

D. Current Stress of Switches

The current stress of switches is a very paramount factor when designing the proposed converter. In nominal state, the current stresses of switches are identically tantamount with those of the conventional converters, but this condition is transmuted for the hold-up time operation. Different from the conventional LLC resonant converter, the proposed converter shows boost PWM operation during the hold-up state. Thus, the peak value and RMS value of the resonant inductor current are varied depending on the obligation ratio of Q_a . Withal, the dc offset current which is represented in the magnetizing inductor affects the current stress of the converter. The dc offset current is calculated utilizing current-second balance rule of the resonant capacitor C_r (optically discern). According to the current-second balance rule of the capacitor, sum of the total charge flows in and out of the resonant capacitor is zero. Therefore, the positive and the negative area in should be identically tantamount. The shaded area of each period, $ta-tb$, $tb-tc$, $tc-td$, $td-te$, and $te-tf$ are expressed as follows:

Shaded area of $ta-tb$

$$\frac{1}{2} X \left(\frac{V_{cr}}{L_r} X I_{Lm} \right) * I_{Lm} \quad (10)$$

E. Reduction of Conduction Loss in the Nominal State

In conventional LLC resonant converters, the converter increases voltage gain by decreasing switching frequencies. Thus, the converter should be designed to be able to operate in wide range



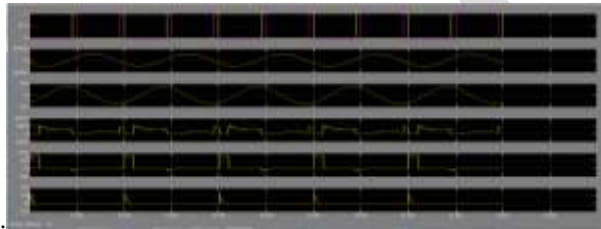
Fig. 8. Maximum current stress of the primary switch (at 75W Specification)

operational principle of the proposed converter in the nominal state is the same as that of the conventional *LLC* resonant converters. The converter is represented as where I_{Lmpk} is the peak value of magnetizing inductor current, t_d is the dead time of the switches, and C_{oss} represents the output capacitance of switches. The high magnetizing inductor current results in conduction loss increases in the converter, so that the magnetizing inductance should be designed to satisfy both conditions, satisfying ZVS condition and minimizing conduction loss increases.

V. SIMULATION RESULTS

To verify the effectiveness of the proposed converter, prototypes of the proposed converter and the conventional *LLC* resonant converter are designed with following 75 W LED TV specifications:

- 1) input voltage range : 250 –400 V;
- 2) hold-up time : 60 ms;
- 3) output voltage : 250 V;
- 4) output power : 75 W (250 V/0.3 A);



- 5) nominal switching frequency: 100 kHz.

Fig.7. Simulation waveforms of the proposed converter operation at minimum input voltage. Nominal state, Hold-up state.

Also, the components used in both converters are the same except the auxiliary switch and the transformers. The auxiliary switch is newly added in the proposed converter. Although the proposed converter does not need any frequency changes for hold-up operation, the same transformer size is used in the experiment because of the dc offset current of the magnetizing Inductor. However, the transformer in the proposed converter can be designed to have higher magnetizing inductance to reduced the RMS value of magnetizing inductor current. Fig. 19 shows the experimental waveforms of the proposed converter both in nominal state operation and hold-up state operation with the minimum input voltage condition ($V_s = 250$ V). As expected, the proposed converter grows up its voltage gain by incrementing the obligation ratio of the auxiliary switch. When no PWM gate signal is applied to the auxiliary switch, the output voltage becomes 153 V and it increments to 250 V for hold-up state operation with 20% obligation ratio of the auxiliary switch Q_a .

The proposed converter shows boost PWM operation during hold-up state and the resonant inductor current is build up to -2.4 A while the auxiliary switch is conducted. The ZVS conditions are achieved in both converters. Since the proposed converter has higher magnetizing inductance, the RMS value and the peak value of the primary current, which is identically tantamount with the resonant inductor current in nominal state operation, is more minuscule in the proposed converter than those of the conventional converter replication is tested by transmuting the operational mode of the proposed converter under the same input voltage condition. Increased voltage gain is represented as the converter changes its operational modes from nominal operation condition to hold-up time operation condition.

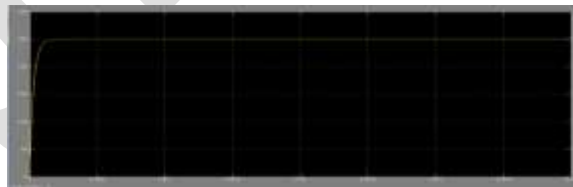


Fig. 9. Simulation waveforms of the proposed converter output voltage.

The proposed converter has higher efficiency over the entire load condition because the loss made by the primary current is reduced in the proposed converter. The efficiency difference becomes maximized at light load condition when the magnetizing inductor current takes up significant portion in the total primary current

VI. CONCLUSION

An incipient HB *LLC* resonant converter having boost PWM operation characteristic has been proposed. By adopting the PWM control method with an auxiliary switch, the proposed *LLC* resonant converter reduces its frequency variation range while maintaining the advantages of the conventional *LLC* resonant converters. Thus, high-K design with high L_m becomes enabled in the proposed converter. It makes the converter have low magnetizing inductor current which results in reduced conduction loss in the proposed converter. The characteristics of the proposed converter are verified with a 75 W prototype and it is compared with the *LLC* resonant

converter. Efficiency increase is represented in the proposed converter over the entire load condition from 0.86% efficiency amendment at full load condition to 3.69% efficiency amelioration at 20% load condition. The efficiency results verifies that the efficacy of the proposed converter and the benefit of the proposed converter becomes maximized at light load condition when the magnetizing inductor current takes a sizably voluminous part in the total primary RMS current value .Consequently, the proposed converter is expected to find wide use for highefficient dc/dc converter having hold-up time requisites

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