# A Switched Capacitor Based Active Z-Network Boost Converter 

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#### Abstract

The voltage gain of traditional boost converter is limited due to the high current ripple, high voltage stress across active switch and diode, and low efficiency associated with large duty ratio operation. High voltage gain is required in applications, such as the renewable energy power systems with low input voltage. A high step up voltage gain DC-DC converter consists of three active Znetworks with switched capacitor technique is proposed in this paper. A distinct advantage of this proposal is that it can reach a high voltage gain without extremely high duty ratio. In addition, the voltage stress of the active switches and output diodes is low. Therefore, low voltage components can be adopted to reduce the conduction loss and cost. The new converter well fulfill the stringent requirements from industry, particularly renewable power systems, to boost low voltage from clean sources such as photovoltaic arrays and fuel cells to high voltages for grid-connected converters. The operating principle and steady-state analysis are discussed in detail. The simulations are conducted to verify the effectiveness of proposed converter in MATLAB/Simulink environment.


Keywords-Boost Converter, Active Z-network, Switched Capacitor, Continuous Conduction Mode . Multilevel, High gain voltage, Reduced voltage stress.

## INTRODUCTION

With the advance of industrial applications, new industries such as the one based on renewable energy have ever higher demands on the power electronics technology. The renewable power systems require dc-dc boost converters to boost low voltages from clean sources such as photovoltaic (PV) arrays and fuel cells to high voltages for the grid-connected inverters. The demand for such a converter can be also found in the back-up energy conversion for uninterruptible power systems, high-intensity discharge lamps for automobile headlamps, the front-end stage for the communication power system[1], to name just a few. In those applications, highly efficient and high step-up dc-dc converters are necessary to handle large input current and sustain high output voltage. Theoretically speaking, the conventional boost converters can realize infinite voltage gain with an extreme duty cycle when ignoring parasitic parameters. Moreover, the conventional boost converters are restricted by the parasitic parameters of their components and suffer serious power loss. Furthermore, the modern semiconductor technology can still not provide efficient and economic high-voltage stress diodes and switches for the boost converters. In practical applications, the voltage gain of the conventional boost converters can maximally reach five to six times of the input voltage, which is far away from the practical requests[2]. To obtain the desired voltage, boost converters can be connected in series, which is, however, very complicated due to the additional switches and control units. Furthermore, the additional switches and control units degrade the reliability of the system. A high-frequency isolation dc-dc converter with a high transformer turn ratio is applied to solve those problems [3], but the efficiency is thus reduced due to the transformer, and the volume and weight of the whole system increase. Some converters can reach high voltage gain by only one or two switches, e.g., a dc-dc multilevel boost converter [4] and a switched-capacitor-based active-network converter[5], but the voltage gain is still not large enough for industrial applications.

A novel, simple, but efficient design was initiated by Peng via applying just an LC network, named as a Z-network, to couple the dc source with the converters, and thus, he proposed a novel source, which is different from the conventional voltage source and current source, and is named as a Z-source[6] .Since then, the Z-source technology has greatly advanced and has distinct advantages, e.g., it can realize a high voltage gain and, meanwhile, can be immune to shoot-through problems. Straight forwardly, to realize a high voltage gain in dc-dc converters, Z-source technologies are also applied to boost the voltage, because Z-source converters can work in the shoot-through mode, and its output voltage can reach a broader range than that of the conventional ones. Peng has proposed some novel Z-source circuits[7],[8] and corresponding control methods[9],[10]. Following Peng's proposals, new Z-source circuits with high voltage gain have also been proposed, such as the algorithms for controlling the converters to reach high voltage gain[11], generalized multicell switched-inductor and switched capacitor Z-source converters for high voltage gain[12], trans-Z-source inverters with the boost function[13], and quasi-Z-source-based isolated dc-dc converters for distributed power generation[14]. However, the voltage gains of these Z-source converters may be still not enough for many industrial applications, which puts forward a challenge for designing converters with even higher voltage gains.

A novel boost converter with three active Z networks is proposed by Zhang et al. [15], which not only have the advantages of the Z-network converters but also can reach much higher voltage gains. Moreover, this 3-Z-network converters operate not only in
continuous current modes (CCMs) but also in discontinuous-current modes(DCMs).However, the voltage stress of the active switches and output diode is very high.

Based on the concept of switched-inductor and switched capacitor[16],[5], this paper proposes a novel switched-capacitorbased active Z-network converter (SC-AZNC) for high step-up conversion, which has the following advantages: high voltage conversion ratio, low voltage stress across switches and diodes, and self-voltage balancing across the output capacitors. The operating principle and steady-state analysis are discussed in detail, and the simulation results are given to verify the analysis.

## SWITCHED CAPACITOR BASED ACTIVE Z-NETWORK

The diagram of the proposed converter is shown in Fig -1, which consists of three active Z-networks and switched capacitor unit. It is different from the traditional Z-source networks, which normally consists of passive elements. In this converter, Z-network1 functions as the first boost part, consisting of inductors $L_{1}$ and $L_{2}$ and diodes $D_{1}, D_{2}$, and $D_{3}$; Z-network 2 is the switch part, consisting of switch Q , capacitor $\mathrm{C}_{1}$, and diodes $\mathrm{D}_{4}$ and $\mathrm{D}_{5}$; and Z-network 3 is the second boost part, consisting of $\mathrm{L}_{3}$ and $\mathrm{L}_{4}$ and diodes $\mathrm{D}_{6}, \mathrm{D}_{7}$, and $\mathrm{D}_{8}$. Multiple capacitors and diodes on the output-stacking form a switched-capacitor unit, with the series or parallel connections between the capacitors, high voltage gain can be achieved. Diodes $\mathrm{D}_{9}, \mathrm{D}_{10}, \mathrm{D}_{11}$ and capacitors $\mathrm{C}_{2}, \mathrm{C}_{3}, \mathrm{C}_{4}$ are adopted in the switchedcapacitor unit.


Fig -1: Switched capacitor based active Z-network boost converter

## Continuous Conduction Mode

Assume that 1) all the components are ideal, 2) the free-wheeling diode of the switch is ignored, and 3) $L_{1}=L_{2}$ and $L_{3}=L_{4}$.
In the periodic states (on and off) of switch Q , the inductor stores and releases energy alternately. Correspondingly, their currents increase and decrease alternately. Then, there correspond some cases to the current states of the inductors as the current decreases to be zero and lasts for an interval, which is called the discontinuous-current case of inductors. Working of the proposed converter is analysed in CCM which then correspond to three modes, i.e., three linear equivalent circuits, as shown in Fig -2(a)-(c), respectively. Therein, $\mathrm{v}_{\mathrm{L} 1}, \mathrm{v}_{\mathrm{L} 2}, \mathrm{v}_{\mathrm{L} 3}$, and $\mathrm{v}_{\mathrm{L} 4}$ are voltages of $\mathrm{L}_{1}, \mathrm{~L}_{2}, \mathrm{~L}_{3}$, and $\mathrm{L}_{4}$, respectively. Assume the clockwise direction as positive directions of the reference currents, and the arrows shown in Fig -2(a) refer to the positive directions of the inductor reference voltages.


Fig -2(a): Mode 1 operation circuit

International Journal of Engineering Research and General Science Volume 3, Issue 4, July-August, 2015


Fig -2(b): Mode 2 operation circuit


Fig -2(c): Mode 3 operation circuit

## Case 1

Case 1: Mode $1 \longrightarrow$ Mode 2. Two modes in this case, namely, Modes 1 and 2, whose equivalent circuits are shown in Fig -2(a) and (b).

Let $i_{L 1}, i_{L 2}, i_{L 3}, i_{L 4}, i_{D 1}, i_{D 2}, i_{D 3}, i_{D 5}, i_{D 6}, i_{D 7}, i_{D 8}, i_{C 1}$, the currents of $\mathrm{L}_{1}, \mathrm{~L}_{2}, \mathrm{~L}_{3}, \mathrm{~L}_{4}, \mathrm{D}_{1}, \mathrm{D}_{2}, \mathrm{D}_{3}, \mathrm{D}_{5}, \mathrm{D}_{6}, \mathrm{D}_{7}, \mathrm{D}_{8}, \mathrm{C}_{1}$, and respectively. $\mathrm{v}_{\mathrm{L} 1}$, $\mathrm{v}_{\mathrm{L} 2}, \mathrm{v}_{\mathrm{L} 3}, \mathrm{v}_{\mathrm{L} 4}, \mathrm{v}_{\mathrm{C} 1}, \mathrm{v}_{\mathrm{C} 2}, \mathrm{v}_{\mathrm{C} 3}, \mathrm{v}_{\mathrm{C} 4} \mathrm{v}_{\mathrm{D} 9}, \mathrm{v}_{\mathrm{D} 10}, \mathrm{v}_{\mathrm{D} 11}$ are the voltages across $\mathrm{L}_{1}, \mathrm{~L}_{2}, \mathrm{~L}_{3}, \mathrm{~L}_{4}, \mathrm{C}_{1}, \mathrm{C}_{2}, \mathrm{C}_{3}, \mathrm{C}_{4}, \mathrm{D}_{9}, \mathrm{D}_{10}$, $\mathrm{D}_{11}$ respectively. Key waveforms for case 1 operation is shown in Fig -3.


Fig -3:Key waveforms of case 1 operation
Mode 1: As shown in Fig -2(a), there are three loops in the circuit, and the arrows in the circuit refer to the current direction in each loop. As Q turns on, diodes $\mathrm{D}_{1}, \mathrm{D}_{3}$, and $\mathrm{D}_{4}$ undertake positive voltages and turn on synchronously; meanwhile, $\mathrm{D}_{2}$ bears negative
voltage and turns off. Thereafter, $L_{1}$ and $L_{2}$ are connected in parallel and then cascaded with $D_{4}, Q$, and $V_{S}$ to form loop 1.The source $V_{S}$ discharges the energy to $L_{1}$ and $L_{2}$, then $i_{L 1}$ and $i_{L 2}$ increase, and $L_{1}$ and $L_{2}$ store the energy. We have,

$$
\begin{gather*}
\mathrm{i}_{\mathrm{D} 1}=\mathrm{i}_{\mathrm{D} 3}=\mathrm{i}_{\mathrm{L} 1}=\mathrm{i}_{\mathrm{L} 2} \\
\mathrm{i}_{\mathrm{D} 2}=0 \\
\mathrm{i}_{\mathrm{D} 4}=\mathrm{i}_{\mathrm{D}}+\mathrm{i}_{\mathrm{D} 3}=2 \mathrm{i}_{\mathrm{L} 1} \\
\mathrm{v}_{\mathrm{L} 1}=\mathrm{V}_{\mathrm{s}} \\
\mathrm{v}_{\mathrm{L} 2}=\mathrm{V}_{\mathrm{s}} \tag{1}
\end{gather*}
$$

Meantime, $D_{5}$ and $D_{7}$ undertake negative voltages and turn off, yet $D_{6}$ and $D_{8}$ endure positive voltages and turn on. Accordingly $L_{3}$ and $L_{4}$ are connected in parallel and then cascaded with $Q$ and $C_{1}$ to form loop 2. $C_{1}$ discharges the energy to $L_{3}$ and $L_{4}$, and $i_{L 3}$ and $i_{L 4}$ increase. Thus $L_{3}$ and $L_{4}$ store energy. We have,

$$
\begin{gather*}
\mathrm{i}_{\mathrm{D} 6 \mathrm{E}} \mathrm{i}_{\mathrm{D} 8=} \mathrm{i}_{\mathrm{L} 3}=\mathrm{i}_{\mathrm{L} 4} \\
\mathrm{i}_{\mathrm{D} 5=0}  \tag{2}\\
\mathrm{i}_{\mathrm{C} 1}=-2 \mathrm{i}_{\mathrm{L} 3} \\
\mathrm{v}_{\mathrm{L} 3=}=\mathrm{v}_{\mathrm{L} 4}=\mathrm{v}_{\mathrm{C} 1}
\end{gather*}
$$

During this time the capacitor $\mathrm{C}_{3}$ is being charged from the capacitor $\mathrm{C}_{2}$, and the energy stored in the capacitors $\mathrm{C}_{2}$, $\mathrm{C}_{4}$ is released to the load.

$$
\begin{equation*}
\mathrm{V}_{\mathrm{C} 2}=\mathrm{V}_{\mathrm{C} 4}=\mathrm{V}_{\mathrm{o}} / 2 \tag{3}
\end{equation*}
$$

Mode 2: At Q turns off, and the mode changes from Mode 1 to Mode 2, as shown in Fig.2.As Q is off, $\mathrm{D}_{1}, \mathrm{D}_{3}, \mathrm{D}_{4}, \mathrm{D}_{6}$, and $\mathrm{D}_{8}$ undertake negative voltage and turn off, yet $D_{2}, D_{5}, D_{7}$, and $D_{9}$ turn on and then form three loops in this mode. Therein, loop 1 is consists of, $\mathrm{V}_{\mathrm{s}}-\mathrm{L}_{1}-\mathrm{D}_{2}-\mathrm{L}_{2}-\mathrm{D}_{5}-\mathrm{C}_{1}$, where $\mathrm{V}_{\mathrm{S}}, \mathrm{L}_{1}$ and $\mathrm{L}_{2}$ discharge energy to $\mathrm{C}_{1}$, namely, $\mathrm{V}_{\mathrm{S}}=\mathrm{v}_{\mathrm{L} 1}+\mathrm{v}_{\mathrm{L} 2}+\mathrm{v}_{\mathrm{C} 1}$. Moreover, $\mathrm{i}_{\mathrm{L} 1}$ and $\mathrm{i}_{\mathrm{L} 2}$ decrease as shown in Fig -3, and the currents of $\mathrm{D}_{2}$ and $\mathrm{D}_{5}$ are equal to $\mathrm{i}_{\mathrm{L} 1}$ for the cascaded connection, and $\mathrm{i}_{\mathrm{C}}$ increases as shown in Fig -3 .We have,

$$
\begin{gather*}
\mathrm{i}_{\mathrm{D} 2}=\mathrm{i}_{\mathrm{D} 5}=\mathrm{i}_{\mathrm{L} 1}=\mathrm{i}_{\mathrm{L} 2} \\
\mathrm{i}_{\mathrm{D} 1}=\mathrm{i}_{\mathrm{D} 3}=\mathrm{i}_{\mathrm{D} 4=0} \\
\mathrm{v}_{\mathrm{L} 1+}+\mathrm{v}_{\mathrm{L} 2}=\mathrm{v}_{\mathrm{S}_{-}-} \mathrm{v}_{\mathrm{C} 1} \tag{4}
\end{gather*}
$$

$V_{S}, L_{1}, D_{2}, L_{2}, D_{5}, L_{3}, D_{7}, L_{4}, D_{9}$, and $C_{2}$ form a loop, where $V_{S}, L_{1}, L_{2}, L_{3}$, and $L_{4}$ discharge the energy to $C_{2}$. $i_{L 3}$ and $i_{L 4}$ decrease .The energy stored in the capacitor $C_{3}$ is released and the capacitor $C_{2}$ and $C_{4}$ are being charged. We have,

$$
\mathrm{v}_{\mathrm{S}}=\mathrm{v}_{\mathrm{L} 1}+\mathrm{v}_{\mathrm{L} 2}+\mathrm{v}_{\mathrm{L} 3}+\mathrm{v}_{\mathrm{L} 4}+\mathrm{v}_{\mathrm{C} 2}
$$

$$
\mathrm{i}_{\mathrm{D} 7}=\mathrm{i}_{\mathrm{L} 3}=\mathrm{i}_{\mathrm{L} 4}
$$

$$
\mathrm{i}_{\mathrm{D} 6}=\mathrm{i}_{\mathrm{D} 8}=0
$$

$$
\mathrm{v}_{\mathrm{L} 3}+\mathrm{v}_{\mathrm{L} 4}=\mathrm{v}_{\mathrm{S}}-\left(\mathrm{v}_{\mathrm{L} 1}+\mathrm{v}_{\mathrm{L} 2}+\mathrm{v}_{\mathrm{C} 2}\right)
$$

$$
\mathrm{v}_{\mathrm{C} 2}=\mathrm{v}_{\mathrm{C} 4}=\mathrm{v}_{\mathrm{o}} / 2
$$

$$
\begin{equation*}
\mathrm{v}_{\mathrm{C} 2}=\mathrm{v}_{\mathrm{C} 3} \tag{5}
\end{equation*}
$$

## Case 2

Case 2:Mode $1 \longrightarrow$ Mode $\longrightarrow \quad$ Mode3. There are three modes in case 2 .due to the direction of $\mathrm{i}_{\mathrm{C} 1}$. i.e., Modes 1,2 and 3, whose equivalent circuits are shown in Fig -2(a)-(c). To describe the operation process of the converter, the key waveforms of the proposed converter in Case 2 are shown in Fig -4. The operation process of the proposed converter in a switch period is analyzed in the following section according to the waveforms in Fig -4

Mode 1: The process is just like the descriptions of Mode 1 in Case 1.
Mode 2: The process is similar to the descriptions of Mode 2 in Case 1 except $\mathrm{i}_{\mathrm{C} 1}$. Therein, $\mathrm{i}_{\mathrm{C} 1}$ decreases as shown in Fig -4 , which is different from the increase of $\mathrm{i}_{\mathrm{C} 1}$ in Fig -3, because the energy stored in the inductors are not enough to charge the load in this case

Mode 3- $\mathrm{i}_{\mathrm{C} 1}$ decreases from 0 to negative, which means that not only $\mathrm{Vs}, \mathrm{L}_{1}$, and $\mathrm{L}_{2}$ but also $\mathrm{C}_{1}$ charge the energy to the following circuit, and they fulfill the same equations as in Case 1.


Fig -4:Key waveforms of case 2 operation

## PARAMETER DESIGN

The parameters of the proposed converter will be discussed according to the analyses above on the operation of the proposed converter in CCM. Normally, the parameters design of a converter is to determine the rated voltages and rated currents of the components in the circuit.

- Output Voltage: According to the analyses of Cases 1 and 2, the output voltage $\mathrm{v}_{\mathrm{o}}$ is as follows.
- Output current:

$$
\begin{equation*}
v_{o}=v_{s} \frac{2(1+D)^{2}}{(1-D)^{2}} \tag{6}
\end{equation*}
$$

$$
\begin{equation*}
I_{\text {in }}=I_{o} \frac{2(1+D)^{2}}{(1-D)^{2}} \tag{7}
\end{equation*}
$$

- Parameters of Inductors: The inductors in the converter can be designed based on the differential equation of inductance. On this basis,

$$
\begin{align*}
& \mathrm{L}_{1}=\mathrm{L}_{2}=\frac{\mathrm{V}_{\mathrm{S}} \mathrm{D}(1-\mathrm{D})^{2} \mathrm{~T}}{\mathrm{x} \% \mathrm{I}_{\mathrm{o}}(1+\mathrm{D})}  \tag{8}\\
& \mathrm{L}_{3}=\mathrm{L}_{4}=\frac{\mathrm{V}_{\mathrm{S}}(1+\mathrm{D}) \mathrm{DT}}{\mathrm{x} \% \mathrm{I}_{\mathrm{o}}} \tag{9}
\end{align*}
$$

- Parameters of Capacitors: The capacitors in the converter can be designed based on the differential equation of capacitance. On this basis,

$$
\begin{align*}
& \mathrm{C}_{1}=\frac{2 \mathrm{I}_{\mathrm{o}} \mathrm{DT}}{\mathrm{x} \% \mathrm{~V}_{\mathrm{S}}(1+\mathrm{D})}  \tag{10}\\
& \mathrm{C}_{2}=\frac{\mathrm{I}_{\mathrm{o}}(1-\mathrm{D})^{2} \mathrm{DT}}{\mathrm{x} \% \mathrm{~V}_{\mathrm{S}}(1+\mathrm{D})^{2}} \tag{11}
\end{align*}
$$

For obtaining self balancing at the output stage assume $\mathrm{C}_{4}=\mathrm{C}_{3}=\mathrm{C}_{2}$.

## SIMULATION RESULTS

To verify the feasibility and validity of the proposed converter, MATLAB/Simulink software is applied for simulation. Assume the parameters of the converter for case 1 operation as follows: $\mathrm{C}_{1}=220 \mu \mathrm{~F}, \mathrm{C}_{2}=\mathrm{C}_{3}=\mathrm{C}_{4}=470 \mu \mathrm{~F}, \mathrm{~L}_{1}=\mathrm{L}_{2}=100 \mu \mathrm{H}, \mathrm{L}_{3}=\mathrm{L}_{4}=200 \mu \mathrm{H}$. Time period for the operation is $10 \mu \mathrm{~s}$. The simulation results are shown in Fig -5.

International Journal of Engineering Research and General Science Volume 3, Issue 4, July-August, 2015 ISSN 2091-2730

(a)

(b)

(c)

(d)

(f)

Fig -5:Simulation Results for case 1 operation

(a)

(b)

(c)

(d)

(e)

(f)

Fig -6:Simulation Results for case 2 operation

Fig $-5(\mathrm{a})$ show the switching signal given to the switch. Duty ratio of the signal is $50 \%$. Fig -5 (b) show the current through the inductor $L_{1}$ and $L_{2}$. Fig -5(c) show the current through the inductor $L_{3}$ and $L_{4}$. Fig $-5(d)$ show the current through the capacitor $C_{1}$. Fig 5(e) show the voltage across the switch. Fig $-5(f)$ show the output voltage.

Assume the parameters of the converter for case 2 operation as follows: $\mathrm{C}_{1}=220 \mu \mathrm{~F}, \mathrm{C}_{2}=\mathrm{C}_{3}=\mathrm{C}_{4}=470 \mu \mathrm{~F}, \mathrm{~L}_{1}=\mathrm{L}_{2}=55 \mu \mathrm{H}, \mathrm{L}_{3}=\mathrm{L}_{4}=$ $155 \mu \mathrm{H}$. The simulation results are shown in Fig -6.

Fig -6(a) show the switching signal given to the switching device. Duty ratio of the signal is $20 \%$.Fig -6(b) show the current through the inductor $L_{1}$ and $L_{2}$. Fig -6(c) show the current through the inductor $L_{3}$ and $L_{4}$. Fig $-6(d)$ show the current through the capacitor $\mathrm{C}_{1}$. Fig -6(e) show the voltage across the switch. Fig -6(f) show the output voltage. The simulation results shows that voltage stress across the switch is half of the output voltage. If we increasing the level of switched capacitor, we can again increase the output voltage and voltage stress across the switch and output diodes is again reduced to a low value .Another main advantage of this circuit is self-voltage balancing across the output capacitor.

## CONCLUSION

This paper has proposed a switched capacitor-based active Z-network converter with high step-up voltage gain, in which only one switch is used. The operating principles of the proposed converter in CCM with two cases according to the state of the capacitor have been discussed in detail. The voltage stress on active switches and diodes is low, which is beneficial to the system efficiency and cost. Since the circuit can reach a high gain voltage, it well fulfill the stringent requirement from industry, particularly renewable power systems, to boost low voltage from clean sources such as PV arrays and fuel cells to high voltages for grid-connected converters. Moreover, the parameters design of the proposed converter has been discussed. Simulations have been conducted to verify the effectiveness of the proposed converter. By using multileval switched capacitor we can again increase the output voltage and educe the voltage stress across the components. It provides a very potential solution for renewable power systems, such as PV converters.

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