International Journal of Engineering Research and General Science Volume 3, Issue 4, Part-2, July-August, 2015
ISSN 2091-2730

Performance Enhancement of Charge Pump using Modified Wilson Current Mirror

Sandhya Save, B.K.Mishra and Jalpaben Pandya

Thakur College of Engineering and Technology, pandyajalpa7@gmail.com, 9561769957

Abstract—Phase locked loops (PLLs) are integral parts of communication devices used in various applications such as frequency synthesizer, clock recovery circuits, synchronization for digital communications, carrier phase, frequency tracking, etc. Charge Pump PLL (CP-PLL) is a type of PLL widely used for today's SoC environment. The non-ideal effects such as jitter, phase noise, reference spur, phase error, etc. influence the CP-PLL performance which significantly affects the performance of the overall system.

Charge Pump is a small but one of the important components of CP-PLL that significantly affects its performance. The Charge Pump circuit generates non-ideal effects such as leakage current, timing mismatch and current mismatch which causes phase error, reference spurs, jitter, etc. at the CP-PLL output.

In this work, the Charge Pump circuit is designed in Matlab Simulink environment to reduce the current mismatch. Simulated results show that current mismatch for the Charge Pump circuit using Modified Wilson current mirror and transmission gate is 1.94% and phase error is also reduced. This set up can be easily utilized to design various Charge Pump to achieve minimum current mismatch for SoC applications.

Keywords—Charge Pump, CAD Tools, Current Mismatch, Current Mirror, Phase Error, Reference Spur, Matlab Simulink

INTRODUCTION

Charge Pump PLL (CP-PLL) is a type of hybrid PLL. CP-PLLs form an integral part of communication systems such as frequency synthesizer, clock recovery circuits, synchronization for digital communications, carrier phase and frequency tracking, etc. CP-PLLs are used for synchronizing the output signal with the input signal in both frequency and phase. The block diagram of CP-PLL is as shown in figure 1. The major building blocks of a CP-PLL are Phase/Frequency Detector (PFD), Charge Pump (CP), Loop Filter (LF) and Voltage-Controlled Oscillator (VCO) [1].

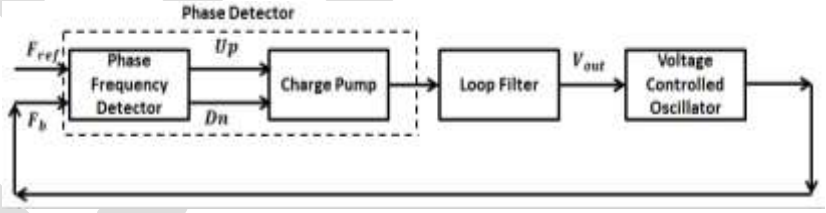

Figure 1: Block diagram of CP-PLL

The Charge Pump (CP) circuit is a small part of CP-PLL which converts the digital error pulses into analog current pulses. The CP circuit plays an important role in determining the CP-PLL performance. The CP circuit consists of two switched current sources I_{UP} (charging current source) and I_{DN} (discharging current source), that pump charge into or out of the LF as shown in figure 2. The capacitor C_p acts as a LF. The inputs to the CP circuit are the Up or Dn signals obtained from the PFD and the output current is coupled to the capacitor C_p. The current sources and switches in CP are usually implemented using MOS transistors. Ideally, the charge pump currents I_{UP} and I_{DN} need to be equal in magnitude but the inherent mismatches between the MOS transistors result in mismatching between the current sources. The mismatch between charging and discharging current is known as current mismatch and it degrades the performance of CP [2].

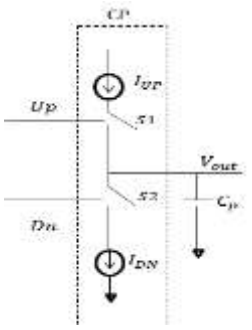

Figure 2: Basic Charge Pump

This mismatch gives rise to phase error and reference spurs in CP-PLL.

The paper is organized as follows. In section 2, phase detector non-idealities are discussed. In section 3, mixed signal CAD tools used for design of phase detector circuit are discussed. In section 4, design of phase detector circuit in Matlab /Simulink /Simscape /Simelectronics environment is presented. In section 5, simulation results are reported and the phase error and reference spurs for the different CP circuits are investigated.

PHASE DETECTOR NON-IDEALITIES

Phase detector circuit exhibits non-ideal behaviour which contributes to phase error and reference spur in CP-PLL [3], [4].

The different non-idealities that occur in phase detector circuit are as given below:

1. Leakage Current

One of the issues in the CP is the leakage current which might be caused by the CP itself, by the on-chip varactor, or by any leakage in the board. This gives rise to change in the output voltage and causes phase error which is given by [3]:

$$\Delta\emptyset leakage = 2\pi \frac{Ileakage}{Icp} (rad) \quad \ldots\ldots (1)$$

Where,

$Ileakage$ - Leakage current occurring in MOS transistors

Icp – CP current

The leakage current is in the order of μA; therefore, the phase error due to leakage current can be ignored.

2. Charge Sharing

The capacitors at nodes ‘a’ and ‘b’ consist of the parasitic source/drain capacitances of MOS transistor. As shown in figure 3, when the switching transistors are open, the charges on the nodes ‘a’ and ‘b’ move towards VDD and GND respectively. When the switches close instantaneously, some of the charge stored on these parasitic capacitors will be transferred to the LF, and cause voltage spikes on the VCO control line. The charge sharing cannot be completely eliminated but it can be reduced by proper design of switches.

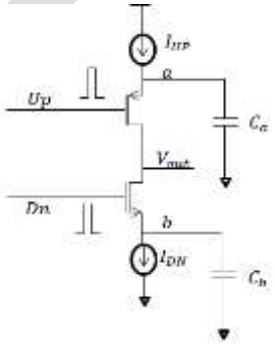

Figure 3: Charge Sharing in CP

3. Clock Feedthrough

When the Up and Dn signals of the MOS switch change their logic levels, due to the overlap of the MOS transistors, some charges are coupled to the LF which causes spikes on the control voltage which leads to reference spurs at the output.

4. Charge Injection

Charge injection is a phenomenon that arises due to leakage of charge into a capacitive node during the turn on and turn off of a switch that is connected to that node. Charge injection and clock feedthrough is directly proportional to gate capacitance.

5. Dead Zone

Dead zone problem occurs when the rising edges of the two clocks to be compared are very close. To mitigate the dead zone issue, the reset signal inside the tri-state PFD as shown in figure 4 needs to be designed carefully as given in equation (2).

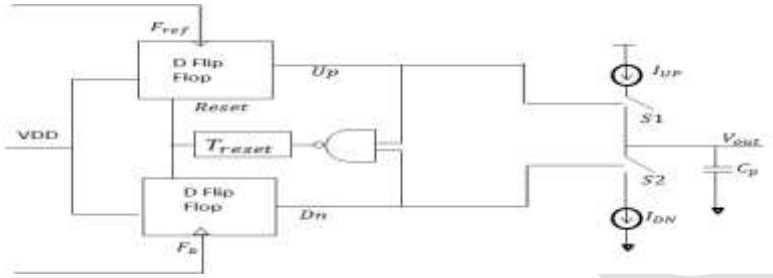

Figure 4: D Flip-Flop based PFD

The reset delay represents the minimum pulse width of the PFD output that is needed to turn on the CP completely.

$$T_{reset} = \frac{1}{(2 \times F_{max})} \quad \ldots\ldots (2)$$

Where,

T_{reset} – Reset Delay in PFD

F_{max} – Maximum operating frequency of PFD

Dead zone contributes to timing mismatch which in turn contributes to phase error and CP non-idealities. Thus, designing a PFD with no dead zone is important for accurate frequency generation, low phase noise in frequency synthesizer PLLs, and low timing jitter in clock generator PLLs.

6. Missing Edge Phenomenon

The PFD suffers from another problem known as missing edge phenomenon. The PFD should provide the clock pulses correctly in the arriving order of the two signals, but it may sometimes miss edges which is known as missing edge phenomenon [5, 6]. This missing edge problem occurs when a rising edge of F_{ref} or F_b signal arrives during the reset delay (T_{reset}) as shown in figure 5.

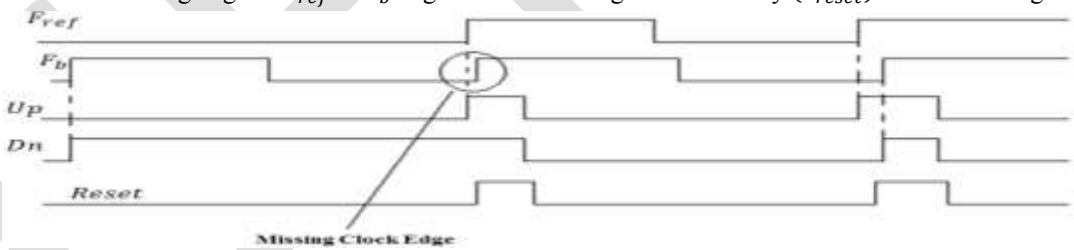

Figure 5: Missing Edge Phenomenon

Some of the rising edges can be missed in the detection when the edges are overlapped with the reset signal internally generated in the PFD, which is called the missing edge problem. Missing edges induce wrong polarity in the PFD output, leading to incorrect behaviour and making the CP-PLL spend more time to acquire phase or frequency. As circuit speed increases, the possibility of missing edges increases.

7. Timing Mismatch

Timing mismatch is inherent with the CP circuit. As the input to the CP is the PFD outputs (Up and Dn) signals; there exists a delay in the PFD outputs reaching the CP. This delay introduces a certain amount of phase error given by [3]:

$$\Delta \emptyset timing = 2\pi \frac{\Delta Tdelay \cdot Ton}{Tref^2} \quad \ldots\ldots (3)$$

Where

$\Delta Tdelay$ - Timing Mismatch in PFD,

$Tref$ - Reference cycle time,

Ton - Turn-on time of the PFD.

In all the previous works, $\Delta Tdelay$ does not consider the switch non-idealities. Therefore, in this work to estimate the non-idealities, the timing mismatch is segregated as given below.

Timing mismatch consists of a) propagation delay between the logical output of PFD and the CP switches, b) Propagation delay for the CP switches to change the state, c) Dead Zone of PFD.

Therefore,

$$\Delta Tdelay = T1 + T2 + T3 \quad \ldots\ldots (4)$$

Where,

$T1$ - Propagation delay due to connection between PFD and CP switch

$T2$ - Propagation delay for the switch to change state

$T3$ - Dead Zone of the PFD

Substituting the values of $\Delta Tdelay$ in equation (3), we get,

$$\Delta \emptyset timing = 2\pi \frac{(T1 + T2 + T3) \cdot Ton}{Tref^2} \ (rad) \quad \ldots\ldots (5)$$

7. Current Mismatch

Current mismatch consists of Mismatch between the drain currents of the current sources. The current sources present in CP are designed using MOS transistors. Due to the inherent mismatches present in transistors such as 2nd order effects and random device mismatches, CP suffers from current mismatches [7]. Current mismatching refers to the magnitude difference of charging and discharging currents. Phase error due to charge pump current mismatch is given by [3]:

$$\Delta \emptyset mismatch = 2\pi \frac{\Delta i}{Icp} \cdot \frac{Ton}{Tref} \ (rad) \quad \ldots\ldots (6)$$

Where,

Icp - Rating current of CPs,

$Tref$ - Reference cycle time,

Ton - Turn-on time of the PFD

Δi - Mismatching of charging and discharging currents

The total phase error $\Delta \emptyset tot$ caused by these non-idealities can be approximated as:

$$\Delta \emptyset tot = 2\pi \ (\Delta \emptyset leakage + \Delta \emptyset mismatch + \Delta \emptyset timing) \quad \ldots\ldots (7)$$

Also, the reference spurs can be given by [4],

$$P_r = 20 \log \frac{N \ F_{bw} \ \Delta \emptyset tot}{\sqrt{2} \ F_{ref}} - 20 \log \left(\frac{F_{ref}}{F_{pl}} \right) \quad \ldots\ldots (8)$$

Where,

P_r – Reference Spur

N - Division ratio of the divider

F_{bw}- Loop Bandwidth

$\Delta \emptyset tot$ – Total Phase Error

F_{ref} – Reference Frequency

F_{pl} - Frequency of the pole in the LF

MIXED SIGNAL CAD TOOL

CP-PLL is a mixed signal block involving the co-design of analog and digital circuits. There are different tools available to design the CP-PLL as shown in table 1 with its advantages and limitations. Referring to table 1, Matlab is a tool which can provide analog and digital design on a common platform [10].

As compared to other tools, Matlab is better for computation than LabVIEW. Simulations execute faster in Matlab (nearly 3 times) as compared to LabVIEW. The maximum error in the delay, computed using Matlab, is less than 8% compared to HSPICE simulation results [8].

Table 1: Mixed Signal Design Tools

S. No	Description	Matlab [8], [9], [10]	Mentor Graphics [10], [11], [12]	Synopsys [10], [13]	Cadence [10], [14],[15]	National Instruments – LabVIEW [10], [16], [17]	Scilab [9],[10],[18], [19]	Oscad [20]
1.	Year of Introduction	1970	1981	1986	1988	1990	2009	2013
2.	Function	Multi-paradigm numerical computing environment	Complete CAD Flow	Complete CAD Flow	Complete CAD Flow	Graphical Programming Environment	Numerical computational package and a high-level, numerically oriented programming language	CAD tool for circuit design, simulation, analysis and PCB design.
3.	Availability	Licensed	Licensed	Licensed	Licensed	Licensed	Open Source	Open Source
4.	AMS Design supported	Yes (Simulink)	Yes (Eldo)	Yes (HSpice)	Yes (Pspice)	Co-Simulation with Matlab	Yes (Scicos)	Yes
5.	MOS Models Supported	Spice model level 1 and 3. Other models can be imported from Pspice.	Supports Eldo level 1-47, 53-70,101 Mosfet models.	Levels 1 to 71	Spice Levels 1 to 7	Spice models can be imported from Pspice, Matlab	In-Built PMOS and NMOS transistors with default parameters is present.	Models can be imported from Ngspice
6.	Programming	Easy	Complex as compared to Matlab	Easy	-	Complex as compared to Matlab	Easy	-
7.	Industry Acceptance	Widely used by scientists and researchers and has good industry acceptance	Moderate	Moderate	Moderate	Moderate	Limited to the developer community	Still in development stage
8.	Co-Simulation	Scilab, Cadence-Pspice, NI-Multisim, Mentor Grpahics-ModelSim, NI-LabVIEW	Matlab	Matlab	Matlab	Matlab, Pspice	Matlab	Ngspice, Scilab

Also, Matlab includes a rich set of plotting capabilities, Matlab help is user friendly and highly descriptive; Matlab GUI is better than other tools. Matlab has a large collection of toolboxes in a variety of domains such as signal processing, communications, image and video processing, control systems, test and measurement, computational finance, etc. One of the key features of this tool is the integration ability with other languages and third-party applications. Therefore, Matlab has become the preferred language of computing for the researchers [10].

Considering the advantages of Matlab environment, the CP and PFD circuit is designed in Matlab Simulink Simelectronics environment.

PHASE DETECTOR DESIGN

The set up for phase detector circuit used in CP-PLL circuit is designed in Matlab Simulink Simelectronics, Spice compatible environment by using 0.18 μm level 3 CMOS model with 3.3V supply as shown in figure 6. The output of the CP is captured on scope as shown in figure 7. The designed CP system is combination of two main sub system PFD and a single ended CP. The subsystem gives the flexibility to reduce the complexity and size of the circuit [21]. The design of sub system PFD is shown in figure 8. The PFD subsystem consists of two edge-triggered, resettable D Flip-Flops (DFF) with their D inputs connected to logic "1". When one of the PFD inputs rises, the corresponding output becomes high. The phase or frequency difference information is stored in the capacitor which is used to tune the VCO.

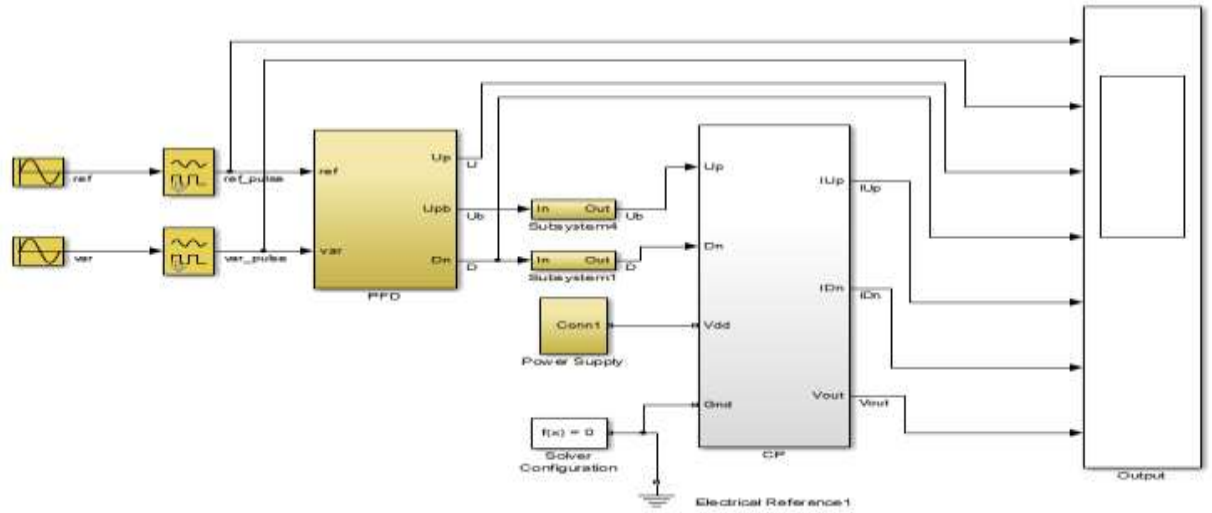

Figure 6: Phase Detector setup used in CP-PLL

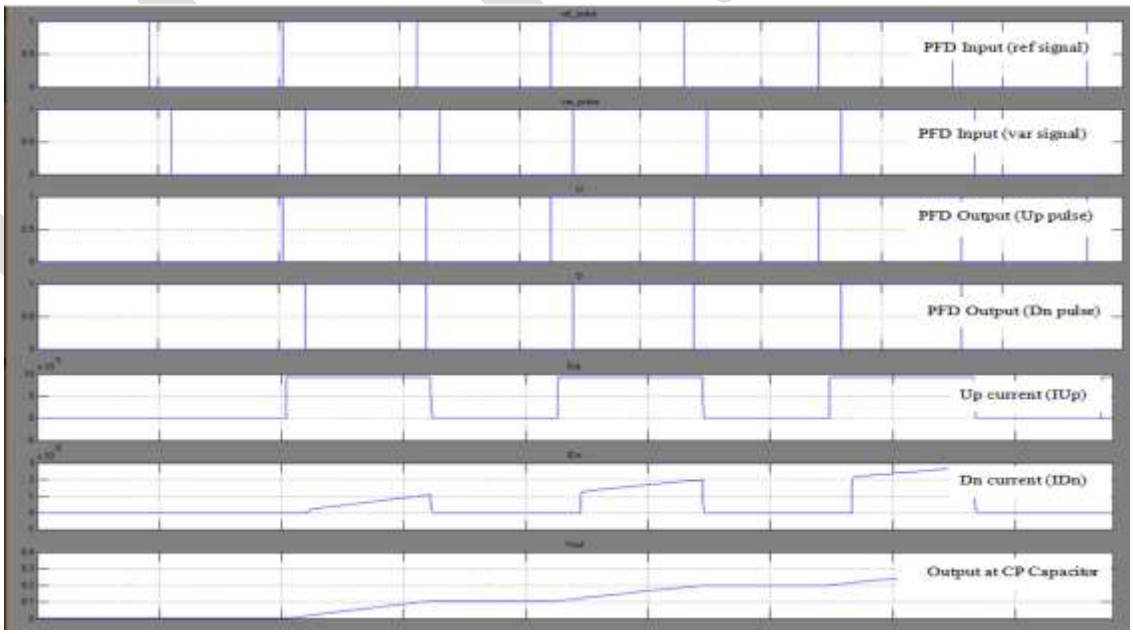

Figure 7: CP response for Reference signal leading Variable signal

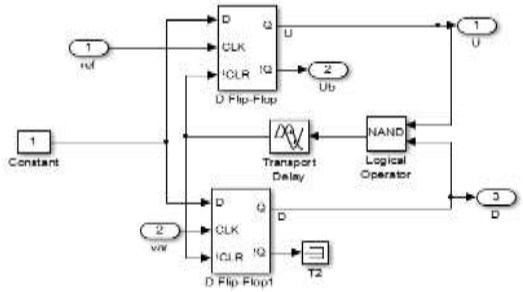

Figure 8: PFD subsystem

The design of single ended CP subsystem is shown in figure 9. CP subsystem consists of PMOS and NMOS current mirror subsystem with Up switch and Dn switch. The current sources in the CP are designed using current mirror circuits [22]. The current mirror circuit uses the principle that if the gate-source potentials of two identical MOS transistors are equal, then the current flowing through their drain terminals should be the same. The charge pump circuits are designed using different combinations of current sources and switches.

1. Basic Current Mirror circuit with PMOS/NMOS switch

In this the CP uses the basic current mirror circuits using PMOS and NMOS transistors (figure 10 and figure 11) whereas the switches used are PMOS and NMOS transistors (figure 12 and figure 13) acting as a switch. The current mismatch caused is estimated as 12.19%.

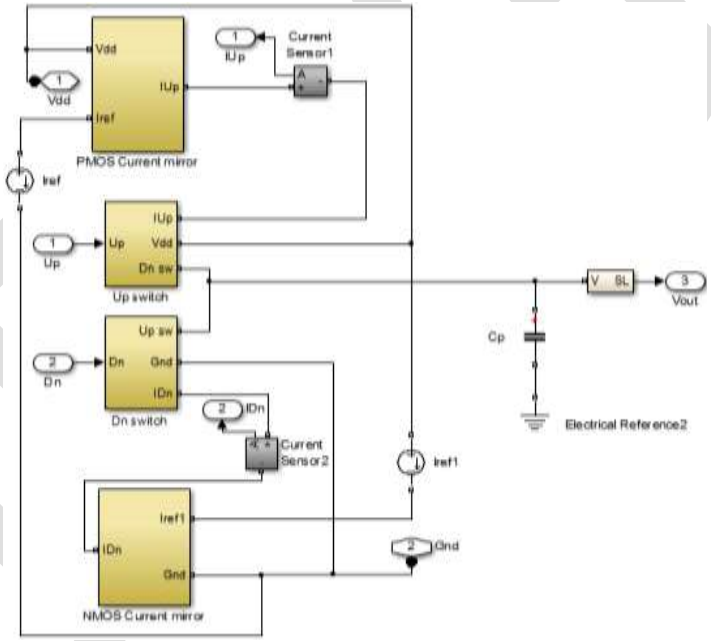

Figure 9: CP subsystem

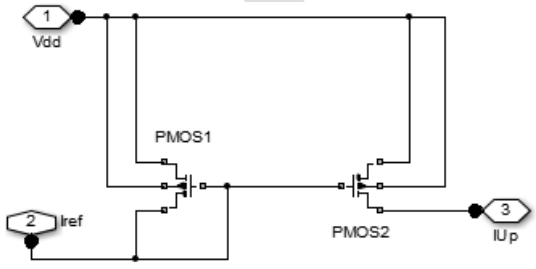

Figure 10: PMOS current mirror subsystem

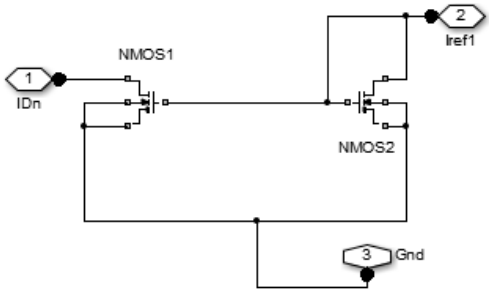

Figure 11: NMOS current mirror subsystem

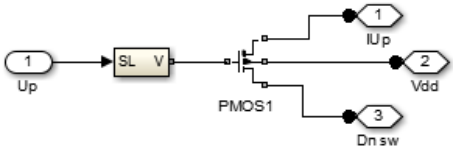

Figure 12: Up switch subsystem

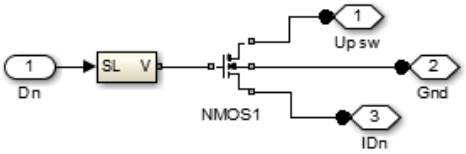

Figure 13: Dn switch subsystem

2. Cascode Current Mirror circuit with PMOS/NMOS switch

As discussed above, the current mismatch can be reduced by increasing the output resistance of the current sources, therefore a Cascode current mirror (figure 14 and 15) is implemented using PMOS/NMOS switch (figure 12 and 13). The current mismatch caused is 10.70%.

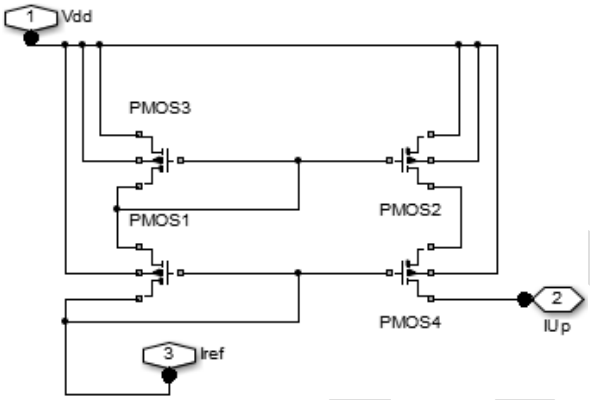

Figure 14: PMOS Cascode Current Mirror

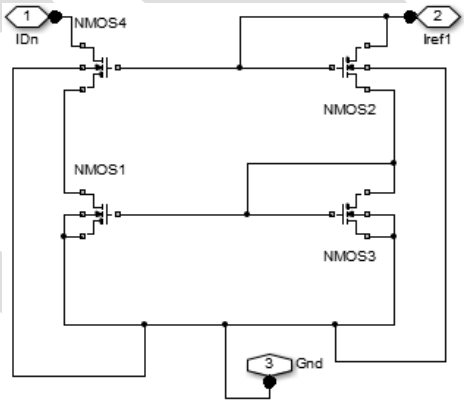

Figure 15: NMOS Cascode Current Mirror

3. Cascode Current Mirror circuit with Transmission gate switch

It is observed that the current mismatch reduces as the output resistance of the current sources increases. To further reduce the charge injection and charge sharing caused due to the PMOS/NMOS switch, a transmission gate (figure 16) is used. The current mismatch caused is 10.06%.

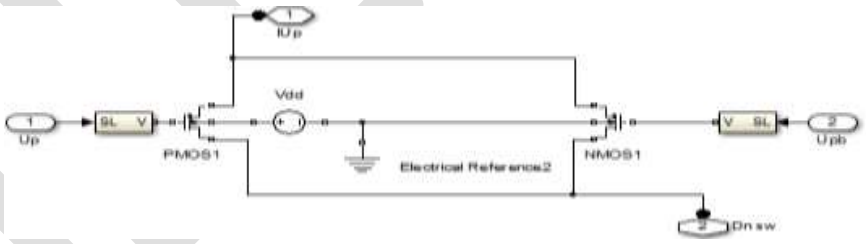

Figure 16: Transmission gate used as a switch in CP circuit

4. Modified Wilson Current Mirror circuit with Transmission gate switch

To further reduce the current mismatch and obtain an improved CP circuit Modified current mirror circuit (figure 17 and 18) is used with transmission gate (figure 16). The current mismatch of the CP is reduced to 6.56%.

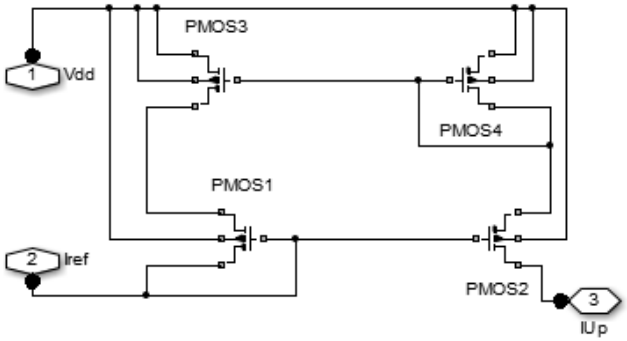

Figure 17: Modified Wilson PMOS Current Mirror

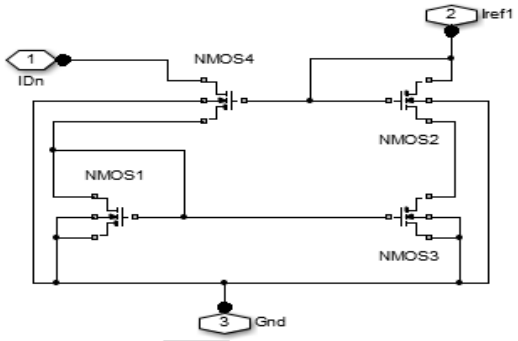

Figure 18: Modified Wilson NMOS Current Mirror

RESULTS AND DISCUSSIONS

When the ref signal leads the var signal, the PFD detects a rising edge on the reference frequency and produces an Up signal. This Up signal from the PFD will turn the Up switch on. This Up pulse will turn on the charging current source and it will cause the CP to inject current into the LF, thus increasing Vout. The obtained simulated result is shown in figure 7.

The designed set up for phase detector of CP-PLL is simulated at 450 MHz with two different current sources and MOS designed switches. The current matching graphs for the different circuits designed are shown in figure 19, 20, 21 and 22 respectively.

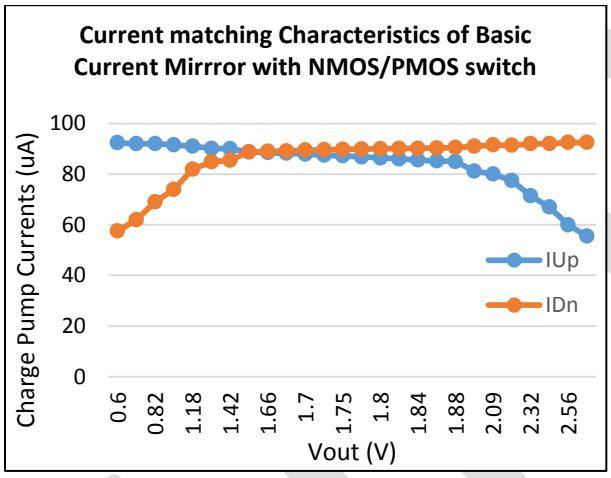

Figure 19: Current matching characteristics of Basic current mirror with PMOS/NMOS switch

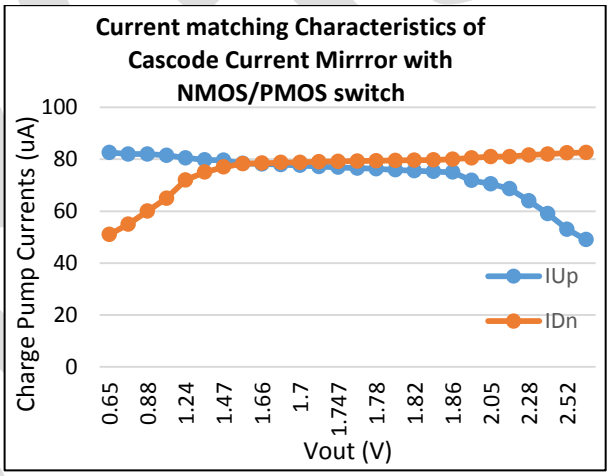

Figure 20: Current matching characteristics of Cascode current mirror with PMOS/NMOS switch

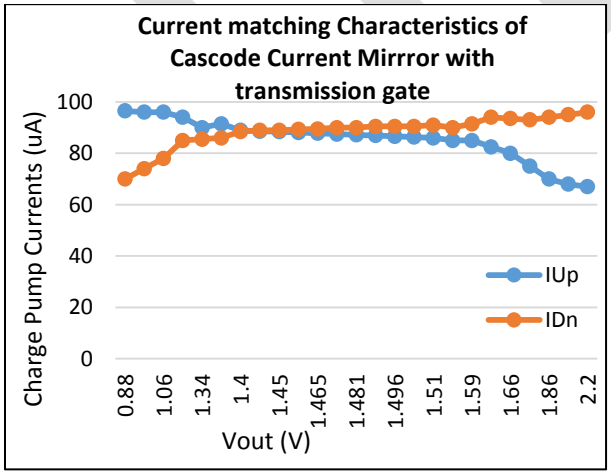

Figure 21: Current matching characteristics of Cascode current mirror with transmission gate

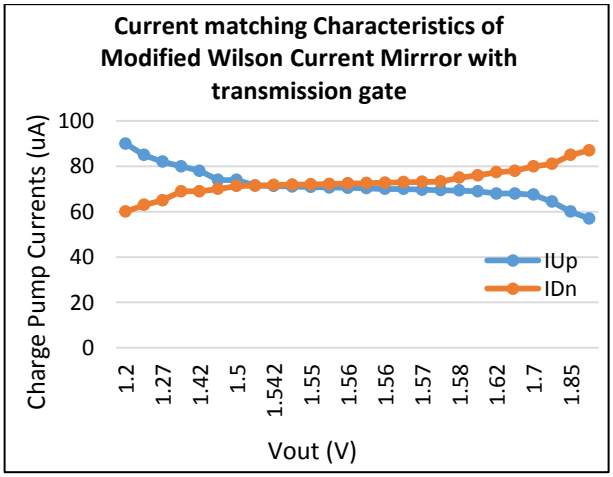

Figure 22: Current matching characteristics of Modified Wilson current mirror with transmission gate

From the graphs it is concluded that current mismatch is reduced for the CP which uses Modified Wilson current mirror with transmission switch. As the PFD circuit suffers from missing edge phenomenon, the PFD circuit is analyzed at different frequencies to estimate the missing edge as shown in table 2.

Table 2. Missing edge Phenomenon at different frequencies and phases

Freq\Phase Diff.	0	10	50	100	150	200	250	300	350
1 MHz	□	□	□	□	□	□	□	□	□
8 MHz	□	□	□	□	□	□	□	□	□
20 MHz	□	□	□	□	□	□	□	□	X
30 MHz	□	□	□	□	□	□	□	□	X
50 MHz	□	□	□	□	□	□	□	□	X
70 MHz	□	□	□	□	□	□	□	□	X
100 MHz	□	□	□	□	□	□	□	X	X
150 MHz	□	□	□	□	□	□	□	X	X
200 MHz	□	□	□	□	□	□	X	X	X
250 MHz	□	□	□	□	□	X	X	X	X
300 MHz	□	□	□	□	X	X	X	X	X
350 MHz	□	□	□	□	X	X	X	X	X
400 MHz	□	□	□	X	X	X	X	X	X
450 MHz	□	□	X	X	X	X	X	X	X

The current mismatch evaluated for the CP using Modified Wilson current mirror circuits and transmission gates is reduced which reduces the phase error and reference spurs. For, this configuration of CP it is found out that the current mismatch is 1.94 μA in the range where no missing edge phenomenon occurs as compared to 14.36 μA in the missing edge phenomenon range at 450 MHz reference frequency. At 230 MHz reference frequency, the current mismatch is 11.78 μA in the range where no missing edge phenomenon occurs as compared to 44.26 μA in the missing edge phenomenon range.

Missing edge phenomenon is not taken into consideration into the previous works. The previous works only focus on reducing the current mismatch by using the op-amp circuits, but at the same time it also increases the area which is a concern for SoC applications. The different designed CP circuits are compared on grounds of Area and Current Mismatch achieved as shown in table 3.

Table 3: Current mismatch in different CP configurations

S. No	CP Circuit	Current Mismatch (%)	Area (μm^2)
1.	Basic Current Mirror with NMOS/PMOS switch	12.19	8.5
2.	Cascode Current Mirror with NMOS/PMOS switch	10.70	23.1
3.	Cascode Current Mirror with Transmission gate	10.06	23.2
4.	Modified Wilson Current Mirror with Transmission gate	6.56*	23.2
		1.94	

*- Count for Missing Edge Phenomenon over all the frequency range

The current mismatch is calculated in table 3 and the timing mismatch is calculated in table 4. Referring to equations 4 and 5, $T1$ is found out to be 100 ps. $T2$ is calculated from different CP circuits and PFD is designed such that no dead zone ($T3$) occurs. But for the worst condition ($T3$) is taken as 100 $e-15$ sec.

Table 4: Timing Mismatch for the different CP configurations

S. No.	Circuit	$T1$ (Propagation delay due to connection between PFD and CP	T2 (Propagation delay for the switch to change	T3 (Dead Zone)	$\Delta Tdelay = T1 + T2 + T3$

		switch)	state)		
1.	Basic Current Mirror with NMOS/PMOS switch	100e-12	2.8e-11	100e-15	1.28e-10
2.	Cascode Current Mirror with NMOS/PMOS switch	100e-12	6.79e-11	100e-15	1.68e-10
3.	Cascode Current Mirror with Transmission gate	100e-12	6.7e-11	100e-15	1.67e-10
4.	Modified Wilson Current Mirror with Transmission gate	100e-12	6.5e-11	100e-15	1.65e-10

Referring table 3 and 4 and referring equations 7 and 8, the phase error and reference spurs are estimated as shown in table 6. From the table it is concluded that the CP using Modified Wilson current mirror and transmission gate achieves reduced current mismatch and occupies less area on chip making it suitable for SoC applications. Therefore, a CP with reduced current mirror is designed and compared with the previous works as shown in table 7 below.

Table 6: Phase error and Reference spur of different CP circuits

S. N.	Circuit	Phase error due to leakage current (rad)	Phase error due to current Mismatch (rad)	Phase error due to timing mismatch (rad)	Reference Spur due to leakage current (dBc/Hz)	Reference Spur due to current mismatch (dBc/Hz)	Reference Spur due to timing mismatch (dBc/Hz)	Total phase error (rad)	Total reference spur (dBc/Hz)
1.	Basic Current Mirror with NMOS/PMOS switch	6.28e-6	0.3480	0.1661	-143.0753	-38.6688	-38.6688	0.5141	-44.8142
2.	Cascode Current Mirror with NMOS/PMOS switch	6.28e-6	0.3054	0.2180	-143.0753	-40.2253	-36.3068	0.5234	-44.6574
3.	Cascode Current Mirror with Transmission gate	6.28e-6	0.2872	0.2167	-143.0753	-40.7611	-36.3587	0.5039	-44.9883
4.	Modified Wilson Current Mirror with Transmission gate	6.28e-6	0.0554	0.2141	-143.0753	-55.0570	-36.4633	0.2695	-50.4241
		6.28e-6	0.1873	0.2141	-143.0753	-44.4749	-36.4633	0.4014	-46.9639*

*- Count for Missing Edge Phenomenon over all the frequency range

Table 7: Comparison with previous works

S. No	Parameters	[23]	[24]	[25]	[26]	This work
1	Process (μm)	0.18	0.18	0.09	0.09	0.18
2	CP Architecture	-	-	Single Ended	Single Ended	Single Ended
3	Supply Voltage (V)	1.8	1	1	1.8	3.3

4	Current Mismatch (%)	- < 1	- < 1	< 6.8	7	1.94*
5	CP current (μA)	100	-	20	-	100
6	Reference Freq. (MHz)	-	-	-	2500	450
7	Area (μm^2)	-	-	-	85.5	23.2
8	Circuit Simulated in	Spectre	Tanner Tool	Spectre	Cadence design environment	Matlab - Simulink environment

*- Count for Missing Edge Phenomenon over all the frequency range

CONCLUSION

A CP circuit design for current mirror and switch reducing current mismatch and phase error is proposed. The complete circuit is designed and simulated in Matlab Simulink Simelectronics in 0.18 um CMOS technology. The current mismatch can be further reduced by employing a feedback which uses operational amplifiers but at the cost of more area and design complexity. Improved current matching reduces the static phase offset and reference spurs of a charge pump PLL. CP circuit using Modified Wilson current mirror improves the performance of charge pump with reduced area. This CP circuit can be used to achieve minimum current mismatch for SoC applications.

REFERENCES:

[1] R. Best, Phase-Locked Loops Design, Simulation, and Applications, Fifth Edition. New York: McGraw-Hill, 2003.
[2] B. Razavi, Design of Analog CMOS Integrated Circuits, McGraw-Hill, New York, NY, USA, 2000, ISBN 0-07-238032-2.
[3] Woogeun Rhee, "Multi-Bit, Delta Sigma Modulation Technique for fractional –N Frequency Synthesizers, University of Illinois, PhD Thesis, 2001.
[4] Li Zhiqun, Zheng Shuangshuang and Hou Ningbing "Design of a high performance CMOS charge pump for phase-locked loop synthesizers," Journal of Semiconductors, vol. 32, no. 7, 2011.
[5] Kangwoo Park and In-Cheol Park, "Fast Frequency Acquisition Phase Frequency Detectors with Prediction-Based Edge Blocking," IEEE Symposium on Circuits and Systems, pp. 1891-1894, 2009.
[6] Mozghan Mansuri, Dean Liu and Chih - Kong Ken Yang, "Fast frequency acquisition phase-frequency detectors for Gsamples/s phase locked loops," IEEE Journal of Solid-State Circuits, vol. 37, no. 10, pp. 1331-1334, 2002.
[7] Marcel J. M. Pelgrom et.al, "Matching Properties of MOS Transistors", IEEE Journal of Solid-State Circuits, vol. 24, No. 5, pp. 1433-1440, 1989.
[8] www.mathworks.com
[9] Comparative Study of Matlab and its Open Source Alternative Scilab: OSSRC Technical Report OSS 0601.
[10] CMC Product Catalogue: http://www.cmc.ca/~/media/NewsAndEvents /BizDev/ Product%20Catalogue%20V30%20V30.pdf
[11] Eldo User's Manual- Software Version 6.8_1 Release AMS 2006.2
[12] www.mentor.com
[13] www.synopsys.com
[14] www.cadence.com
[15] www.orcad.com
[16] http://www.ni.com/labview/
[17] Tadej Tasner, Darko Lovrec, Francisek Tasner and Jorg Edler, "Comparison Of Labview and Matlab For Scientific Research," Annals of the Faculty of Engineering Hunedoara - International Journal of Engineering, vol. 10, no. 3, pp. 389-394, 2012.
[18] http://www-rocq.inria.fr/scilab/
[19] http://pdfoiogv.org/k-440974.html
[20] http://www.oscad.in/resource/book/oscad.pdf
[21] B. K. Mishra, Sandhya Save and Rupali Mane, "A Novel Method to Design Analog Circuits Using Simulink," Proceedings published by International Journal of Computer Applications, pp. 6-13, 2011.
[22] D.R. Holberg P.E.Allen. CMOS Analog Circuit Design. New York: Oxford University Press, 2002.\
[23] Jae Hyung Noh and Hang Geun Jeong, "Charge pump with a regulated cascode circuit for reducing current mismatch in PLLs," Proceedings of World Academy of Science, Engineering and Technology, vol. 25, pp. 185-187, 2008.
[24] J.S. Lee, M.S. Keel, "Charge pump with perfect current matching characteristics in phase-locked loops," Electronics Letters, no. 36, pp.1907–1908, 2000.

[25] L.F. Tanguay, M. Sawan, Y. Savaria, "A very-high output impedance charge pump for low-voltage low-power PLLs," Microelectronics Journal, vol. 40, no. 6, pp. 1026-1031, 2009.

[26] Umakanta Nanda, Debiprasad Priyabrata Acharya and Sarat Kumar Patra, "A New Transmission Gate Cascode Current Mirror Charge Pump for Fast Locking Low Noise PLL," Circuits, Systems, and Signal Processing, vol.33, no. 9, pp. 2709–2718, 2014