International Journal of Engineering Research and General Science Volume 3, Issue 4, Part-2, July-August, 2015
ISSN 2091-2730

A Voltage Quadruple DC-DC Converter with PFC

Cicy Mary Mathew, Kiran Boby, Bindu Elias

P.G. Scholar, cicymary@gmail.com , +91-8289817553

Abstract— A two inductor, interleaved power factor corrected converter exhibiting voltage quadruple characteristic is introduced. The proposed converter operates at a duty cycle more than 50%. The input P.F is improved along with reduced voltage stress Across the semiconductor devices. Also a high voltage gain is obtained almost 4 times that of a conventional boost converter. The simulation are carried out for 25 V AC input in MATLAB/SIMULINK 2010a, to justify the properties of the proposed converter

Keywords— Volt-sec balance, High voltage gain, Voltage quadruple, power factor, active PFC, Ripple cancellation, interleaved converter

INTRODUCTION

To meet the challenges of ever-increasing power densities of today's AC/DC power supplies, designers are continuously looking for opportunities to maximize the power-supply efficiency, minimize its component count, and reduce the size of components. Full-bridge diode rectifier has long been used in AC/DC conversion due to its simple and robust circuit. A single DC/DC converter, which is connected after the rectifier, is then able to perform power factor correction (PFC) and output voltage regulation .When an electric load has a PF lower than 1, the apparent power delivered to the load is greater than the real power that the load consumes. Only the real power is capable of doing work, but the apparent power determines the amount of current that flows into the load, for a given load voltage. Power factor correction (PFC) is a technique of counter acting the undesirable effects of electric loads that create a power factor PF that is less than 1. Most of the research on PFC for nonlinear loads is actually related to the reduction of the harmonic content of the line current. There are several solutions to achieve PFC. There are two types of PFC 1) Passive PFC 2) Active PFC. The Active PFC is further classified into low-frequency and high-frequency Active PFC depending on the switching frequency.

The block diagram of power supply with Active PFC network is shown in figure. 1. Here we see it has an active PFC and a DC DC converter which works as a power conditioner and the load is connected. The load may be a DC load or an AC load connected through an inverter.

The operating principle of the proposed circuit is explained in detail in the following sections The circuit is divided into two sections : the PFC stage and the converter stage. Design of the components is also explained briefly in the third section. Section 4 shows the simulation results.

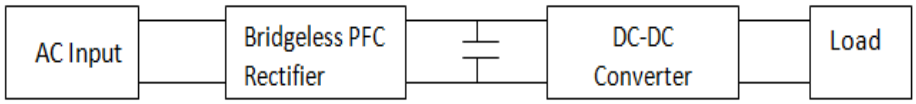

Figure.1 : Block diagram of power supply with an Active PFC

OPERATING PRINCIPLES

An Active power factor correction makes the load behave like a resistor leading to near unity load power factor and the load generating negligible harmonics. The input current is similar to the input voltage waveform's wave shape. The proposed circuit consists of an input PFC stage connected to a boost DC DC converter via a DC link. The figure 1shows the block diagram of power supply with an Active PFC.

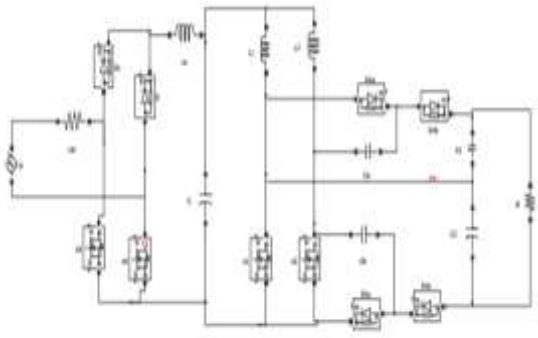

Figure. 2: Circuit diagram of the proposed DC DC converter with PFC

A bridgeless PFC circuit is used in the proposed circuit. In a conventional PFC rectifier, the output ground is always connected to the AC source through the full-bridge rectifier whereas, in the bridgeless PFC rectifier in Figure3, the output ground is connected to the AC source only during a positive half-line cycle, through the body diode of switch S_2, while during a negative half-line cycle the output ground is pulsating relative to the AC source with a high frequency (HF) and with an amplitude equal to the output voltage. This High Frequency pulsating voltage source charges and discharges the equivalent parasitic capacitance between the output ground and the AC line ground, resulting in a significantly increased common-mode noise. An inductor is connected at the DC side, the current through which is continuous for a large value of L_a.

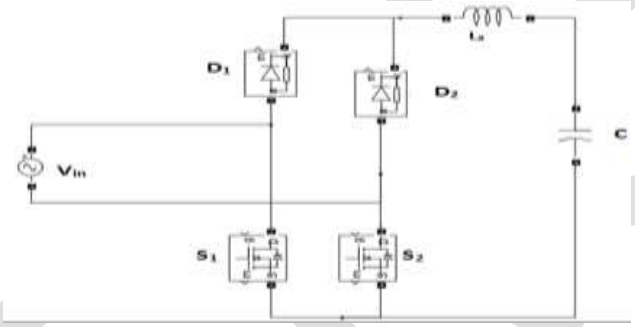

Figure3. Active PFC Stage

The rectified output from the AC-DC PFC stage is stored in a DC-Link capacitor. This capacitor Acts like an input to the DC-DC boost converter stage. A voltage quadrupler DC-DC converter is used in this stage. This converter is so named as the gain is almost four times the gain of a conventional boost converter. The circuit is as shown in figure.4.

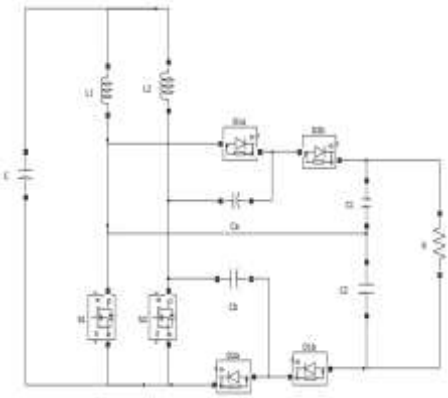

Figure. 4: DC-DC boost converter stage

The operation of this converter can be explained through its four operating modes. It has two switches S_1 and S_2, the switching signals of whose are 180^o out of phase with each other. The modes of operation of this converter is explained below.

1) *Mode I ($t_0<t<t_1$)*: The switches S_1 and S_2 are ON, D_{1a},D_{1b},D_{2a},D_{2b} are all OFF. The corresponding equivalent circuit is shown in Figure.5. From figure.5, it is seen that both i_{L1} and i_{L2} are increasing to store energy in L_1 and L_2, respectively. The voltages Across diodes D_{1a} and D_{2a} are clamped to capacitor voltage V_{CA} and V_{CB}, respectively, and the voltages Across the diodes D_{1b} and D_{2b} are clamped toV_{C2} minus V_{CB} andV_{C1} minus V_{CA}, respectively. Also, the load power is supplied from capacitors$C_1$and C_2.

2) *Mode II ($t_1<t<t_2$)* : For this operation mode, switch S_1 remains conducting and S_2 is turned OFF. Diodes D2a and D2bbecome conducting. The corresponding equivalent circuit is shown in Figure.6. It is seen from Figure.6 that part of stored energy in inductor L_2as well as the stored energy of C_A is now released to output capacitor C_1 and load. Meanwhile part of stored energy in inductorL_2 is stored in C_B. In this mode, capacitor voltageV_{C1} is equal to V_{CB} plus V_{CA}. Thus, ,i_{L1} still increases continuously and i_{L2} decreases linearly.

3) *Mode III ($t_3<t<t_4$) :* For this operation mode, both S_1 and S_2 are turned ON. The corresponding equivalent circuit turns out to be the same as Figure.7

4) *Mode IV ($t_4<t<t_5$) :* For this operation mode, switch S_2 remains conducting and S1 is turned OFF. Diodes D_{1a} and D_1 become conducting. The corresponding equivalent circuit is shown in Figure.8 It is seen from Figure. 8 that the part of stored energy in inductor L_1 as well as the stored energy of C_B is now released to output capacitor C_2 and load. Meanwhile, part of stored energy in inductor L_1 is stored in C_A. In this mode, the output capacitor voltageV_{C2} is equal to V_{CB} plus V_{CA}. Thus, i_{L2} still increases continuously and i_{L1} decreases linearly.

The equivalent theoretical waveforms of currents and voltages for the afore said modes is shown in figure9. Note that the voltage Across switches is low and also the circuit exhibits automatic current sharing without any need of extra circuitry.

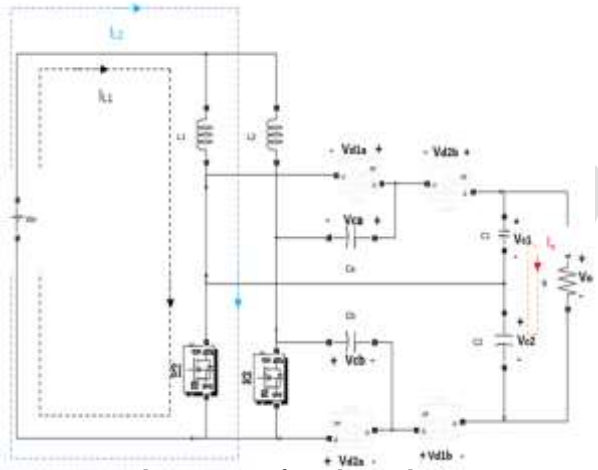

Figure.5: Equivalent circuit of Mode 1and 3 operation

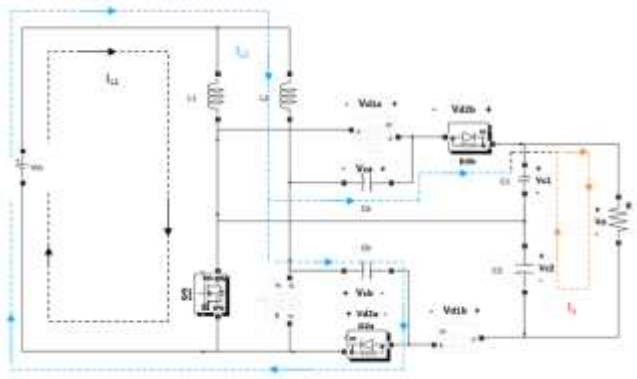

Figure.6: Equivalent circuit of Mode 2 operation

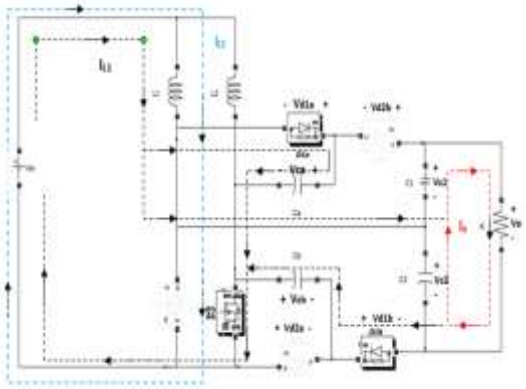

Figure7 :Equivalent circuit of Mode 4 operation

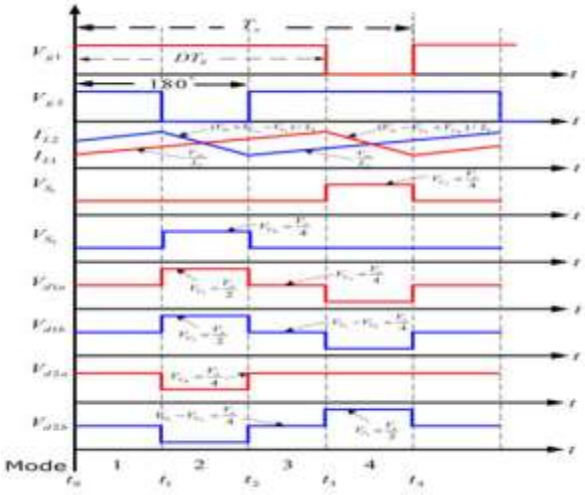

Figure 8: Theoretical Waveforms

DESIGN OF COMPONENTS

The value of the Input filter inductor , DC link capacitor , input inductors, blocking capacitors and output capacitors can be found by the equations discussed in subsection below.

The value of the inductor appropriate for proper working of the converter can be decided by the voltage sec balance of the inductor current. From voltage-sec balance principle

$$\Delta i_{L1} = \frac{V_{in} D T_s}{L_1} \qquad (1)$$

Since $L_1 \approx L_2$, therefore

$$\Delta i_{l2} = \frac{V_{in} D T_s}{L_2} \qquad (2)$$

Thus, for:
Vin = 25V D = 0.75 Ts
Let us assume a standard acceptable value of ΔI_L as 2.4A. we get $L_1 \approx L_2 \approx$ 197.5H

The value of the capacitor appropriate for proper working of the converter can be decided by the charge balance of capacitor. The voltage Across the capacitor is approximately constant. Hence, the voltage ripple ΔVc is taken to be a very small value approximately 0.1V. The equations for the capacitor value are:

$$C_a = I_c + I_L\left(\frac{1-D}{\Delta V_C} T_s\right) \qquad (3)$$

Since $C_a \approx C_b$ therefore

$$C_b = I_c + I_L\left(\frac{1-D}{\Delta V_C} T_s\right) \qquad (4)$$

Thus we get the values as $C_a \approx C_b \approx 30\mu F$

The value of the capacitor appropriate for proper working of the converter can be decided by the charge balance of capacitor. The voltage across the capacitor is approximately constant. Hence, the voltage ripple, 4Vc is taken to be a very small value approximately 0.1V The equations for the capacitor value are:

$$C_2 = I_c + I_L(\frac{1-D}{\Delta V_C} T_s) \quad (5)$$

Since $C_1 \approx C_2$ therefore

$$C_2 = I_c + I_L(\frac{1-D}{\Delta V_C} T_s) \quad (6)$$

Thus we get the values as $C_1 \approx C_2 \approx 250$ µF

From the equivalent circuits of mode 1 and mode 2 , we can get the relationship between the output voltage and voltage Across output capacitors as

$$V_o = V_{c1} + V_{c2} = \frac{4V_{in}}{1-D} \quad (7)$$

Thus the voltage gain of the converter, M is

$$M = \frac{V_o}{V_{in}} = \frac{4}{1-D} \quad (8)$$

To simplify the voltage stress analyses of the components of the proposed converter, the voltage ripples on the capacitors are ignored. The voltage stresses on Active powers switches $S_3$and S_4 can be obtained directly as shown in the following equation:

$$V_{s3max} = V_{s2\max} = \frac{V_o}{4}$$

Hence the voltage stress of Active switches of the converter is equal to one fourth of the output voltage, which enables one to adopt lower voltage rating devices to further reduce both switching and conduction losses. Also, from the equivalent circuits of mode 1 and 2 operation, the circuit voltage stress of diodes D_{1a}, D_{1b}, D_{2a} and D_{2b} can be obtained directly be written as:

$$V_{D1amax} = V_{D1b\max} = V_{D2bmax} = \frac{V_o}{2}$$

$$V_{D2amax} = \frac{V_o}{4}$$

SIMULATION RESULTS

The proposed circuit was simulated in MATLAB/SIMULINK. The AC input given was 25V, peak to peak. It is fed through a bridgeless PFC rectifier. Figure 10 shows input current . Figure11 shows the voltage Across DC link. The value of inductor chosen is 300µH and capacitor value is 30µF. The inductors L_1 and L_2 are chosen as 190µH. The blocking capacitors, C_a and C_b are chosen as 30µF and output capacitors, C_1 and C_2 are chosen as 250µF. MOSFET is chosen as switch. Switches S_1 and S_2 work at 40kHz switching frequency at 75% duty cycle. For the positive cycle only switch S_1 works while S_2 works for negative half cycle. Similarly the Switches S3 and s4 work at 40 kHz switching frequency and with 75% duty cycle. The signal to switches S_3 and S_4 are 180^o out of phase with each other. Figure10 shows the Simulink model. Figure14 to figure19 show the low voltage stresses on the semiconductor devices.

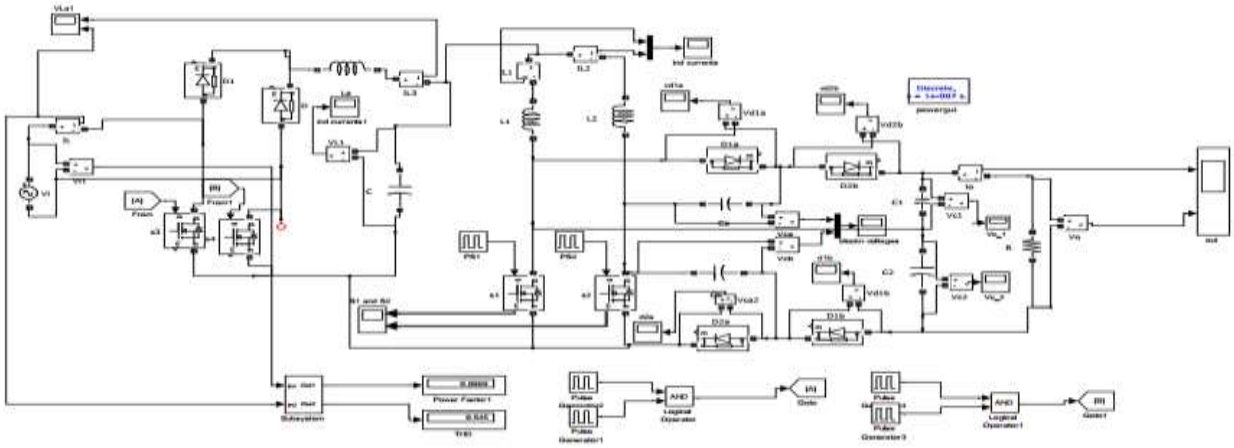

Fig.9 Simulation diagram

Fig 10 shows the input current waveform . From this we see that the input current is almost in phase with the input voltage. Therefore the power factor is nearer to unity. The simulation value of pf 0.98. also the input harmonic distortion is less than 40 percent.

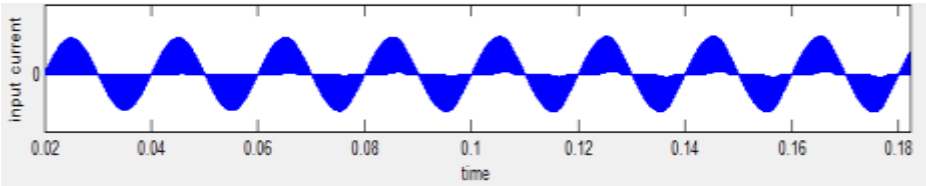

Figure.10: Input A.C. Current

Figure 11 shows the DC link voltage. This voltage is the input to the boost converter section. For an input of 25 V A.C about 21.33V dc link voltage is obtained.

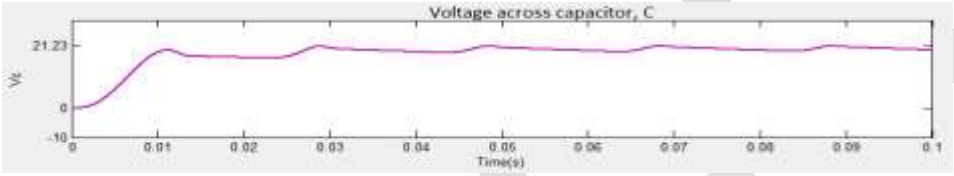

Figure.11: Voltage Across DC-Link Capacitor.

Figure 12 shows the inductor currents . From the result it is clear that input current ripple cancellation is taking place in effect as both the currents are seen to be in 180^{o} phase shift.

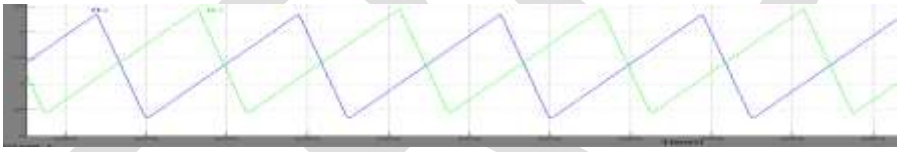

Figure 12: Inductor currents I_{l1} and I_{l2}

Figure 13 shows the output voltage. For a 25V A.C input a 325.33 output DC voltage is obtained.

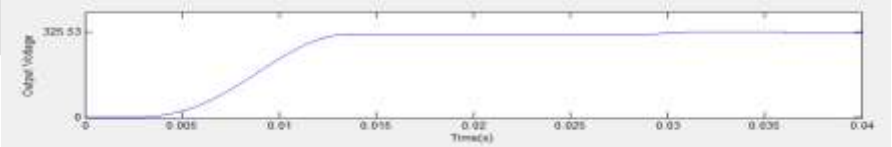

Figure. 13 Output Voltage

Figure 14 to 17 show the voltage across diodes D_{1a} D_{1b} D_{2a} and D_{2b} respectively. From the results it is clear that the maximum voltage across D1a, D1b, D2b is $V_o/2$, whereas the maximum voltage across D_{2a} is $V_o/4$. This justifies the low voltage stress across diodes.

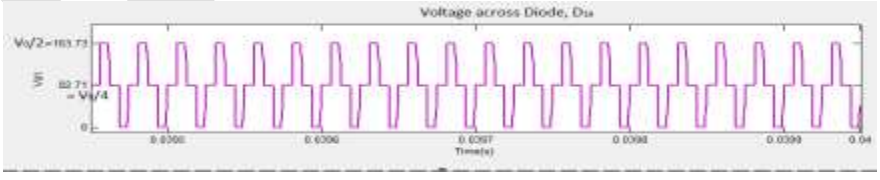

Figure. 14 Voltage Across Diode D_{1a}

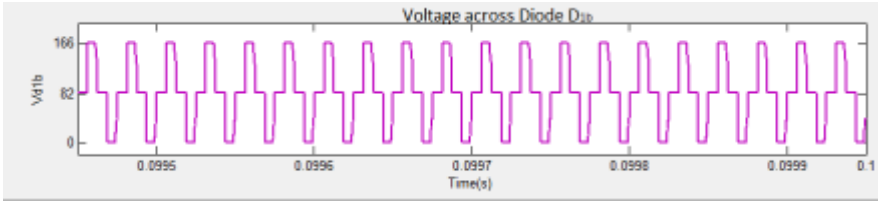

Figure. 15 Voltage Across Diode D_{1b}

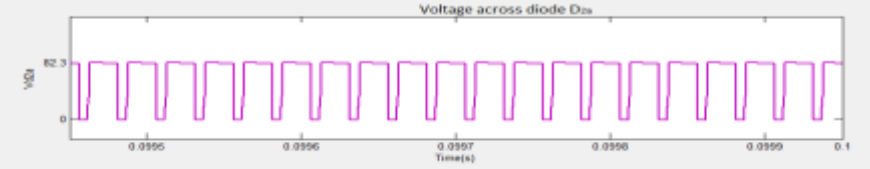

Figure. 16 Voltage Across Diode D_{2a}

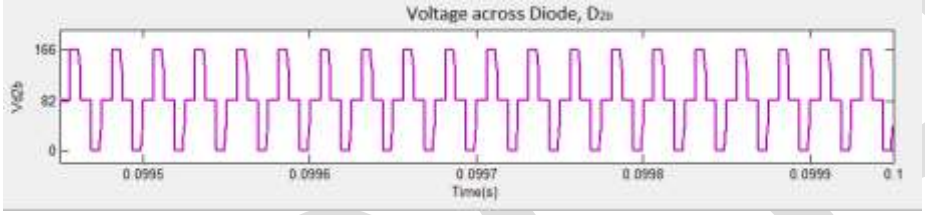

Figure. 17 Voltage Across Diode D_{2b}

Figure 18 and 20 show the voltage across switches S_1 and S_2 respectivelty. From the results it is clear that the maximum voltage across S1, S2 is $V_o/4$. This justifies the low voltage stress across switches.

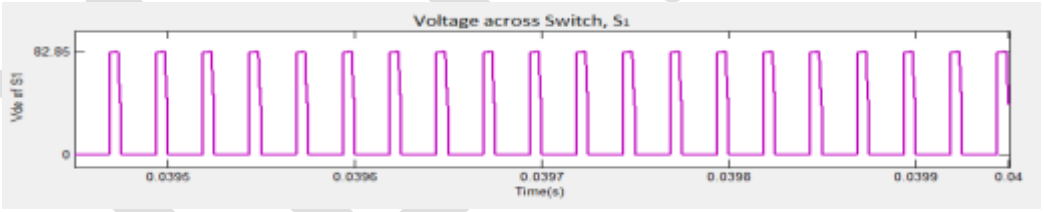

Figure. 18 Voltage Across Switch S_1

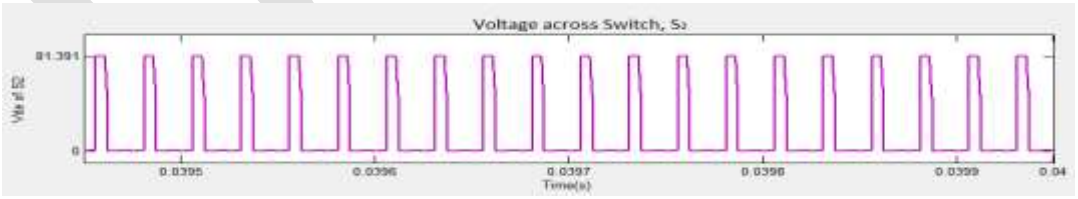

Figure. 19 Voltage Across Switch S_2

CONCLUSION

The proposed circuit was simulated in MTALAB/SIMULINK210a and the results were verified. For an input of 25V AC, a 325.33 V output was obtained. The input power factor obtained was approximately nearer to unity about 0.98 and THD found was 54%. The steady state analysis was done. The voltage Across semiconductor devices is low. The voltage stress Across switches is ¼ th the output voltage and that of the diodes D1a D_{1b}, D_{2b} is $V_0/2$ while that for diode D_{2a} is $V_0/4$. Also a high gain output is obtained. Therefore the proposed circuit can be used at applications where a PFC and high gain are required.

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