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Design Of High Resolution PC Based Data Acquisition System

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Abstract— The main objective of this paper is to design a PC based data acquisition system with a high resolution of 16 bits which can be currently used as an add on DAQ module to make measurements in the range of microvolts. This paper describes the design considerations to be taken into account for selection of components such as ADC, Microcontroller etc. so that it can also be further extended for measurement of time in sub microseconds.

Keywords- Resolution, ADC, Aperture Delay, Architecture, Microcontroller, Selection, Design, IsolatedRS-485, sub-microseconds.

INTRODUCTION

Data acquisition is the process by which physical phenomena from the real world are transformed into electrical signals that are measured and converted into a digital format for processing, analysis, and storage by a computer. [1]
In a Data acquisition system the real-world signals physical phenomenon or physical property such as temperature, light intensity, gas pressure, fluid flow, force etc. is measured. Regardless of the type of physical signal to be measured it is first transformed into an electrical form such as voltage by sensors and transducers.

A data acquisition system can be functionally divided into two parts:
(1) The Analog Front End (AFE)
(2) Digital Signal Processing

The analog front end comprises of the signal conditioning hardware which makes the signal suitable to interface it to the Analog to Digital Convertor (ADC). It consists of comparators, Operational amplifiers, filters, switches, electrical isolators, sensors and actuators, etc. Some DAQ devices include built-in signal conditioning designed for measuring specific types of sensors.

The second section of the circuit i.e the digital signal processing comprises of ADC, microcontroller, memory, drivers etc. This portion digitizes signals, processes the signal to meaningful units, scales acquired signal and calibrates overall system to minimize errors and display the results. The DAQ hardware may communicate results to PC. The key to the effective application of PC-based data acquisition is the careful matching of real world requirements with appropriate hardware and software. Monitoring data can be as simple as connecting a few cables to a plug-in board and running a menu-driven software package.

The objective of this paper is to design a high resolution DAQ system which can be used as a general purpose add on module for measurement of any physical parameter which is converted to voltage. The measured signal is further processed and data is sent to PC via Isolated RS-485 communication protocol. Data acquisition with a PC enables one to display, log, further process and control variables. This system has been designed keeping in mind that it can be extended further for measurement of time in sub microseconds range.

SYSTEM DESIGN

The basic elements of a data acquisition system, as shown in Figure 1, are as follows:
1) Transducers/Sensors
2) Signal conditioning
3) ADC
4) Microcontroller
5) Memory
6) PC

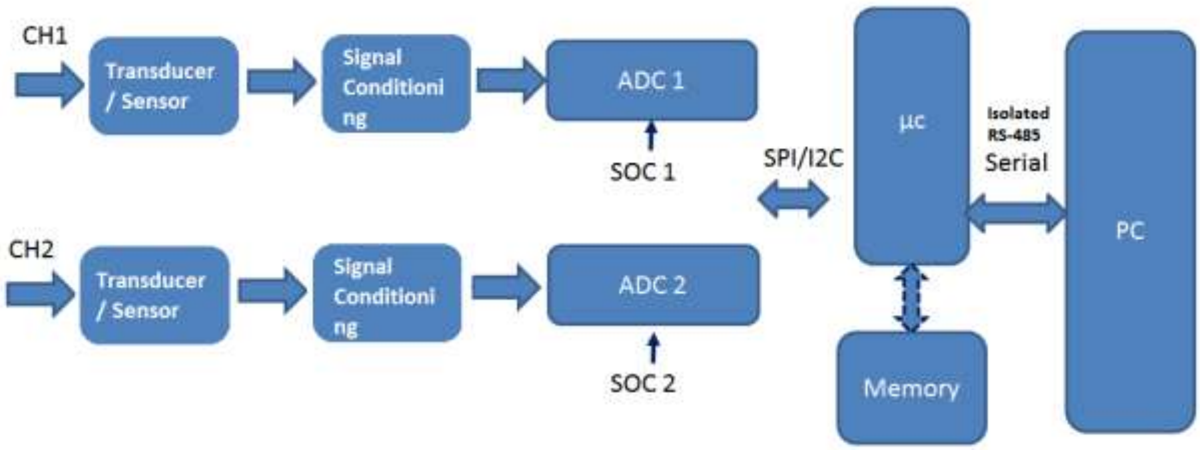

Fig.1. System Architecture

Each block of the total system is important for the accurate measurement and collection of data from the process or physical phenomena being monitored [1]. We focus on each block in the following sections:

1.1 Transducers and sensors and signal conditioning

Transducers and sensors provide the actual interface between the real world and the data acquisition system by converting physical phenomena into electrical signals that the signal conditioning and data acquisition hardware can accept. Transducers available can perform almost any physical measurement and provide a corresponding electrical output. [1]

In electronics, signal conditioning means manipulating an analog signal in such a way that it meets the requirements of the next stage for further processing. [2] Signal conditioning includes amplification, filtering, converting, range matching, isolation and any other processes required to make sensor output suitable for processing after conditioning.

1.2 ADC

Selecting the proper ADC for a particular application appears to be a formidable task, considering the thousands of converters currently on the market.[3] It is based on more than just the precision or bits.[4]

As this circuit is designed keeping in mind it would be further extended for sub microsecond measurement, ADC becomes the most crucial part of the design for capturing the correct instant of the signal.

There are various factors to be considered for selecting ADC. These are listed as follows:

(1) Resolution
(2) Aperture Delay
(3) Aperture jitter
(4) Acquisition time
(5) Conversion time
(6) ADC Architecture
(7) Type of references

The importance of these parameters is elaborated as below:

1.2.1. Resolution:
Smallest change in the digital output that can be detected corresponding to a change in analog input. Higher the ADC resolution, better the time resolution for sub microseconds measurement.
It is important to always design a system to allow for more bits than initially required [4]: if an application calls for 12 bits of accuracy, choose a 16-bit converter. The achievable accuracy of a converter will generally be less than the total number of bits available.

1.2.2. Aperture Delay:

Aperture delay is the measure of the acquisition performance. It is the time between the rising edge of the Convert input and when the input signal is held for a conversion.[5] (Sample to hold delay)
This is one of the most crucial parameter for ADC selection. Sub microseconds measurements require ADC with minimum aperture delay in the rang e of nano seconds.

1.2.3. Aperture jitter:

The sample-to-sample variation in aperture delay is called aperture jitter. It results from the noise superimposed from the hold command and causes corresponding voltage error. It is usually measured in rms.[6] A maximum of few picoseconds tolerance can be permitted .for Sub microseconds measurements.

1.2.4. Acquisition Time:

Acquisition time is the time required to charge and discharge the holding capacitor on the front end of an ADC. [5]
It is the maximum time required to acquire a new input voltage once a sample command has been given. (Hold to sample time)
This parameter becomes crucial when the time difference between the inputs arriving at the same channel is extremely small.

1.2.5. Conversion Time:

The time required for the A/D converter to complete a single conversion once the convert command has been given to the ADC.
Again, this parameter becomes crucial when the time difference between the inputs arriving at the same channel is extremely small;

1.2.6. Differential non-linearity (DNL)

In an ideal A/D converter, the midpoints between code transitions should be 1 LSB apart. Differential non-linearity is defined as the deviation in code width from the ideal value of 1 LSB. Therefore, an ideal A/D converter has a DNL of 0 LSB, while practically this would be ± l/2 LSB. If DNL errors are large, the output code widths may represent excessively large or small ranges of input voltages. Since codes do not have a code width less than 0 LSB, the DNL can never be less than –1 LSB. In the worst case, where the code width is equal to or very near zero, then a missing code may result. This means that there is no voltage in the entire full-scale voltage range that can cause the code to appear. In Figures 2 and 3, the code-width of code 0110 is 2 LSBs, resulting in a differential non-linearity of +l LSB. As the code-width of the code 1001 is 1/2 LSB, this code has a DNL of –1/2 LSB. In addition, the code 0111 does not exist for any input voltage. This means that code 0111 has –1 DNL and the A/D converter has at least one missing code.

Often, instead of a maximum DNL specification, there will be a simple specification of monotonicity or no missing codes. For a device to be monodic, the output must either increase or remain constant as the analog input increases. Monotonic behavior requires that the differential non-linearity be more positive than –l LSB. However, the differential nonlinearity error may still be more positive than +1 LSB. Where this is the case, the resolution for that particular code is reduced.[1]

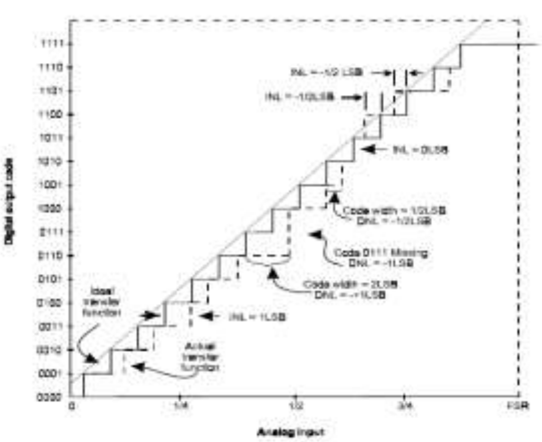

Fig.2. Integral non-linearity errors specified as low-side transition

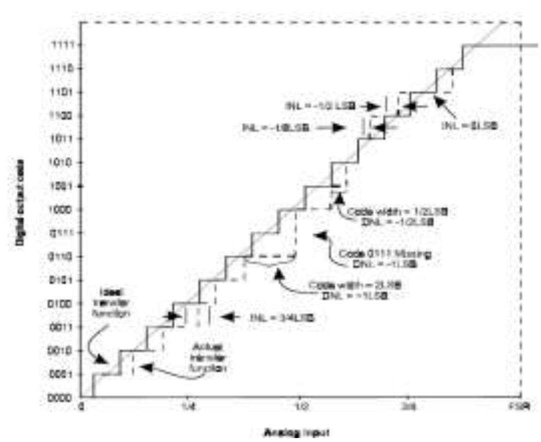

Fig.3. Integral non-linearity errors specified as high-side transition

1.2.7. Integral non-linearity (INL)

This is the deviation of the actual transfer function from the ideal straight line. This ideal line may be drawn through the points where the codes begin to change (low-side transition or LST), as shown in Figure2 , or through the center of the ideal code widths (center-of code or CC), as shown in Figure 3. Most A/D converters are specified by low-side transition INL. Thus, the line is drawn from the point 1/2 LSB on the vertical axis at zero input to the point 3/2 LSB beyond the last transition at full-scale input. The deviation of any transition from its corresponding point on that straight line is the INL of the transition. In Figure 2, the transition to code 0100 is shifted to the right by 1 LSB, meaning that the LST of code 0100 has an INL of +l LSB. In the same figure the transition to code 1101 is shifted left by 1/2 LSB, meaning that the LST of code 1101 has an INL of –l/2 LSB. When the ideal transfer function is drawn for center-of-code (CC) integral non-linearity specification, as shown in Figure 3, the INL of each transition may be different. Where the digital code 1101 previously had –1/2 LSB of LST INL, it now has 0 LSB of CC INL. Similarly, the code 1011 has –1/8 LSB of CC INL, where it previously had 0 LSB of LST INL. The INL is an important figure because the accurate translation from the binary code to its equivalent voltage is then only a matter of scaling. [1]

1.2.8. ADC Architecture:

Selecting the right ADC architecture is important as it decides the performance and successful implementation of the system to a great extent.

Following are a few most widely used ADC architectures with their peculiar characteristics and the reason behind not using a particular architecture:

1.2.8.1. *Continuous Sampling Sigma Delta* – This architecture is generally used for signals which are of continuous type and slowly varying in nature such as temperature.

1.2.8.2. *Dual slope* – This architecture is eliminates the power line noise of 50Hz / 60Hz and conversion time which is quite large.

1.2.8.3. *Flash* – Generally flash ADCs have a maximum resolution of 10 bits which is low. Our objective is to design a high resolution ADC.

1.2.8.4. *Successive Approximation (SAR)* – They are instantaneous sampling type of ADCs, have Low conversion time, and good resolution upto 20 bits as compared to other ADCs. Also SAR ADCs can be used for a wide range of the applications because of its moderate characteristics for most type of signals.

1.2.9. Type of Reference:

All ADCs need to have the same full scale and hence the same reference. Individual internal references can have tolerance which would directly affect the accuracy of readings and therefore an ADC with external refrence should be used.

Considering all the above factors we select high resolution 16 bit SAR ADC which has got aperture delay in nano seconds, jitter in pico seconds and conversion time in micro seconds which would be good enough for most of the applications and also system can be further extended for sub micro seconds measurement.

1.3 Microcontroller

The microcontroller is probably the most popular choice for stand-alone systems, as it provides the necessary peripheral functions on chip. The advantages of microcontrollers include reduced cost, a reduction in chip count and hence reduction in printed circuit board 'real estate'.[1]Choosing a microcontroller from a number of different microcontrollers is a very important for the designers. Three are the vital major criteria for selecting them. These are
(a) wide availability and reliable sources
(b) meeting the requirements efficiently and cost effectively
(c) availability of the software development tools like compilers, Assemblers and debuggers etc. [7]

The other important criteria for selecting microcontroller are:

1. Controllers Architecture
2. Memory type
3. No. of digital and analog I/O's
4. Power consumption
5. Speed of processing
6. Availability
7. Manufacturers support
8. Inbuilt communication interfaces available
9. No. of Interrupts available
10. Additional features such as RTC, capacitive inputs , PWM outputs, Timers etc.

In this particular application keeping in mind the system extension we would select a microcontroller has to carry out the following major functions:

1. Communicate and synchronize with multiple ADCs to obtain digitized data on SPI/I2C port.
2. Store the obtained data in buffer memory.
3. Calibrate the system to minimize errors.

4. Scale values in time domain.
5. Communicate the calibrated and scaled values for display on PC using Serial port.

The factors taken into consideration while selecting Microcontroller***:***

1. Inbuilt SPI/I2C communication modules on which the ADC communicates and UART module in order to communicate the values to PC.
2. High clock rate for fast processing.
3. Enough Memory to store calibration factors, scaling factors and buffered data.
4. On chip real time debugging capability for easy troubleshooting.
5. Low power consumption so that system could be battery operated in future.
6. Small size to make system compact and portable.
7. On board programming.
8. Code protection for security purpose.
9. It should have an internal FRAM memory to store nonvolatile data such as calibration constants. In case it doesn't have provision for the same, an external E2PROM can be interfaced.

The system is programmed for the following basic logic shown in Fig.4. Once all independent inputs are connected to channels, the ADC conversion begins on rising edge of convert pulse. Once data is converted, it is sent to microcontroller for further processing. This data transmission from ADC to microcontroller takes place one channel at a time. After all values are read, The stored offset count is applied ,voltage value is calculated and displayed on PC.

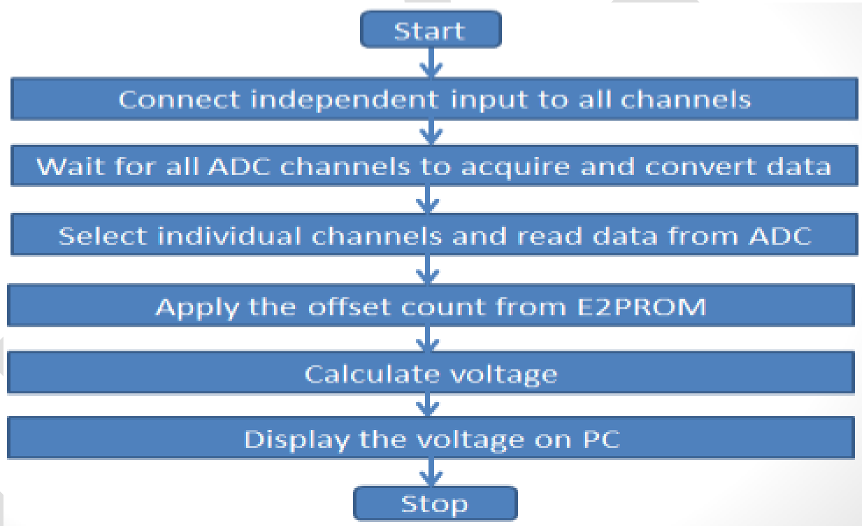

Fig.4. The Program Flow

1.4 Communication interface with PC

The advent of smart instrumentation such as digital transmitters and their use in a distributed data acquisition and control system, the requirements of interfacing multiple devices on a multi-drop network has led to the extensive use of the RS-485 communications interface.[1]

The EIA RS-485 is the most versatile of the EIA standards, and is an expansion of the RS-422 standard. The RS-485 standard was designed for two-wire, half duplex, balanced multi drop communications, and allows up to 32 line drivers and 32 line receivers on the same line. It incorporates the advantages of balanced lines with the need for only two wires (plus signal common) cabling.[1]

RS-485 provides reliable serial communications for:
· Distances of up to 1200 m
· Data rates of up to 10 Mbps
· Up to 32 line drivers permitted on the same line
· Up to 32 line receivers permitted on the same line

The RS-485 interface standard is very useful for data acquisition and control systems where many digital transmitters or stand-alone controllers may be connected together on the same line. Special care is taken in software to co-ordinate which devices on the network become active. Where there is more than one slave device on the network, the host computer acts as the master, controlling which transmitter/receiver will be active at any given time.[1]

The use of RS-485 multi-drop networks greatly reduces the amount of cabling required because each signal conditioning module shares the same cable pair. It does however require an RS-232 to RS-485 converter to allow communications between the computer and the remote signal conditioning modules.[1]

Tha main advantage of using an isolated RS-485 interface is that the PC is protected in case there is problem in the DAQ card.

RESULTS

The designed circuit is implemented successfully for measurement of voltages in with resolution microvolts. Table 1. shows the set voltage value, calculated ADC count, the obtained ADC count, the voltage obtained by scaling ADC count, Percentage error of reading and Percentage error of the entire range of 5 V.

Table.1. Output for the designed system having low percentage error

Sr.No.	Set Value	Calc count	Obatined Count	Obatined Voltage	% Err reading	%Err range
	(V)			(V)	%	%
1	0.00233	30	30	0.00228	2.020	0.001
2	0.50492	6616	6616	0.5049	0.004	0.000
3	1.00469	13165	13166	1.00477	-0.008	0.000
4	1.4999	19654	19655	1.49998	-0.005	-0.002
5	2.0001	26208	26211	2.0003	-0.010	-0.004
6	2.5	32759	32762	2.50025	-0.010	-0.005
7	3.0001	39312	39316	3.00042	-0.011	-0.006
8	3.5008	45873	45876	3.50113	-0.009	-0.007
9	4	52414	52416	4.00015	-0.004	-0.003
10	4.504	59018	59005	4.503	0.022	0.020
11	4.9949	65448	65452	4.99501	-0.022	-0.022

It can be seen from the results that after calibration percentage error is very low and 16 bit high resolution system can measure input voltage with a very high accuracy.

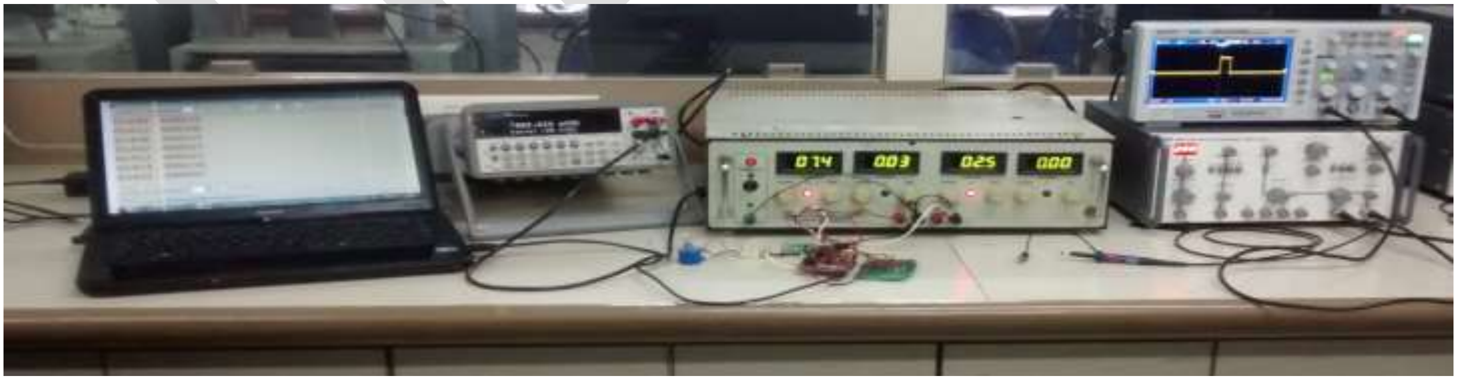

Fig.5. The Entire testing set-up

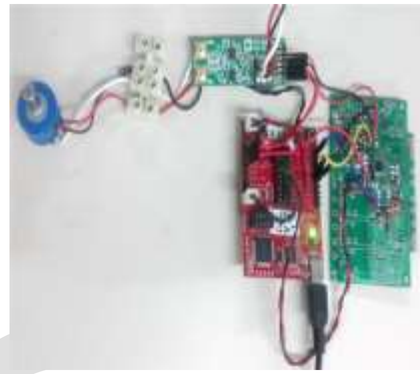

Fig.6. The set voltage on 6 and ½ digit multimeter and obtained ADC counts and voltage on PC

Fig.7. The test boards

Fig.5. shows the entire testing setup which includes the boards, 6 and ½ digit multimeter, Power supplies, oscilloscope and function generator. In Fig.6. we see that the voltage shown on the 6 and ½ digit multimeter which is the set voltage is same as the acquired voltage from the board, shown on PC. The PC displays two columns; first columns the obtained ADC count and the second column is the voltage calculated from that count. Fig.7. is the test board for this project.

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CONCLUSION

The results obtained from this high resolution system have very low Percentage error. This general board can incorporate variety of measurements such as Thermocouple, thermistor, RTD, by incorporating some scaling/formulas/logic etc. as it is highly accurate. The selected ADC is capable to capture instantaneous data with a high resolution of 16 bits. This system is designed keeping in mind it can be extended for measurement of time in sub microseconds. The microcontroller with good memory, inbuilt modules and on chip debugging capability proves to be vital. The isolated RS-485 helps to make the PC safe by separating ground in case of any damage to the card and makes multi-dropping possible.

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