

An efficient Grid tie Solar PV based Single Phase Transformer less Inverter on common mode voltage analysis

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Abstract - The paper presents common mode voltage analysis of single phase grid connected photovoltaic inverter. Many researchers proposed different grid tie inverters for applications like domestic powering, street lighting, water pumping, cooling and heating applications. Traditional grid tie PV inverter uses either a line frequency or a high frequency transformer between the inverter and grid. The transformer provides galvanic isolation between the grid and the PV system but it also offers large inductive reactance to the grid which intern results in increased impedance of line. In order to increase the efficiency, to reduce the size and cost of the system, the effective solution is to remove the isolation transformer but it leads to appearance of common mode (CM) ground leakage current due to parasitic capacitance between the PV panels and the ground. The common mode current reduces the efficiency of power conversion stage, affects the quality of grid current, deteriorate the electric magnetic compatibility and give rise to the safety threats. In order to eliminate the common mode leakage current in Transformerless PV system, the proposed converter utilizes two split ac-coupled inductors that operate separately for positive and negative half grid cycles. This eliminates the shoot-through issue that is encountered by traditional voltage source inverters, leading to enhanced system reliability. SPWM technique and Phase disposition (PD) PWMs are implemented for common mode voltage and THD comparisons, it is observed that PD is efficient in eliminating common mode voltage and reduced THD output. The proposed system is analyzed using MATLAB/SIMULINK software.

Keywords: Common Mode Leakage Current, Transformerless grid connected PV Inverter, unipolar SPWM.

1. Introduction

Grid tie photovoltaic (PV) systems, particularly low-power single-phase systems up to 5 kW, are becoming more important worldwide. They are usually private systems where the owner tries to get the maximum system profitability. Issues such as reliability, high efficiency, small size and weight, and low price are of great importance to the conversion stage of the PV system [1]–[3]. Quite often, these grid-connected PV systems include a line transformer in the power-conversion stage, which guarantees galvanic isolation between the grid and the PV system, thus providing personal protection. Furthermore, it strongly reduces the leakage currents between the PV system and the ground, ensures that no continuous current is injected into the grid, and can be used to increase the inverter output voltage level [1], [2], [4]. The line transformer makes possible the use of a full-bridge inverter with unipolar pulse width modulation (PWM). The inverter is simple. It requires only four insulated gate bipolar transistors (IGBTs) and has a good trade-off between efficiency, complexity and price [5].

Due to its low frequency, the line transformer is large, heavy and expensive. Technological evolution has made possible the implementation, within the inverters, of both ground-fault detection systems and solutions to avoid injecting dc current into the grid. The transformer can then be eliminated without impacting system characteristics related to personal safety and grid integration [1], [4], [6]–[8]. In addition, the use of a string of PV modules allows maximum power point (MPP) voltages large enough to avoid boosting voltages in the conversion stage. This conversion stage can then consist of a simple buck inverter, with no need of a transformer or boost dc–dc converter, and it is simpler and more efficient. But if no boost dc–dc converter is used, the power fluctuation causes a voltage ripple in the PV side at double the line frequency. This in turn causes a small reduction in the average power generated by the PV arrays due to the variations around the MPP. In order to limit the reduction, a larger input capacitor must be used. Typical values of 2 mF for this capacitor limit the reduction in the MPPT efficiency to 1% in a 5-KW PV system [8]. However, when no transformer is used, a galvanic connection between the grid and the PV array exists. Dangerous leakage currents (common-mode currents) can flow through the large stray capacitance between the PV array and the ground if the inverter generates a varying common-mode voltage [1], [4]

Recently, several transformerless inverter topologies have been presented that use super junction MOSFETs devices as main switches to avoid the fixed voltage-drop and the tail-current induced turn-off losses of IGBTs to achieve ultra high efficiency (over 98% weighted efficiency) One commercialized unipolar inverter topology, H5, as shown in Fig.1, solves the ground leakage current issue and uses hybrid MOSFET and IGBT devices to achieve high efficiency. The reported system peak and CEC efficiencies with an 8- kW converter system from the product datasheet is 98.3% and 98%, respectively, with 345-V dc input voltage and a 16-kHz switching frequency.[9-11]

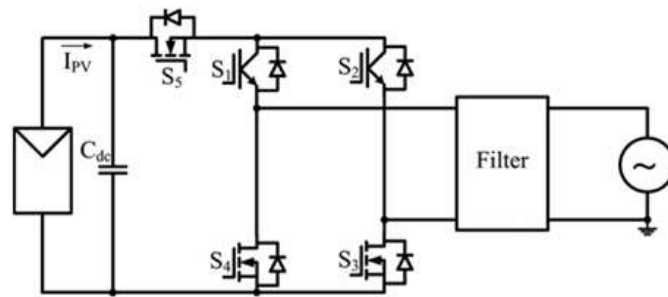


fig 1. Single-phase transformerless PV inverters using super junction MOSFETs H5 circuit

However, this topology has high conduction losses due to the fact that the current must conduct through three switches in series during the active phase. Another disadvantage of the H5 is that the line-frequency switches S1 and S2 cannot utilize MOSFET devices because of the MOSFET body diode's slow reverse recovery. The slow reverse recovery of the MOSFET body diode can induce large turn-on losses, has a higher possibility of damage to the devices and leads to EMI problems. Shoot-through issues associated with traditional full bridge PWM inverters remain in the H5 topology due to the fact that the three active switches are series-connected to the dc bus. Replacing the switch S5 of the H5 inverter with two split switches S5 and S6 into two phase legs and adding two freewheeling diodes D5 and D6 for freewheeling current flows, the H6 topology was proposed is shown in fig.2[11-12]

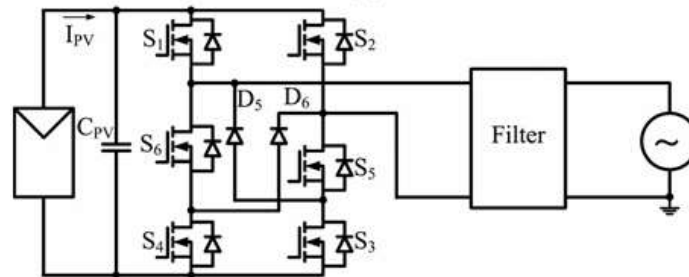


fig.2 Single-phase transformerless PV H6 inverters

The H6 inverter can be implemented using MOSFETs for the line frequency switching devices, eliminating the use of less efficient IGBTs. The reported peak efficiency and EU efficiency of a 300 W prototype circuit were 98.3% and 98.1%, respectively, with 180 V dc input voltage and 30 kHz switching frequency. The fixed voltage conduction losses of the IGBTs used in the H5 inverter are avoided in the H6 inverter topology improving efficiency; however, there are higher conduction losses due to the three series-connected switches in the current path during active phases. The shoot-through issues due to three active switches series connected to the dc-bus still remain in the H6 topology. Another disadvantage to the H6 inverter is that when the inverter output voltage and current has a phase shift the MOSFET body diodes may be activated. This can cause body diode reverse-recovery issues and decrease the reliability of the system.

Another high efficiency transformerless inverter topology is the dual paralleled-buck converter, as shown in Fig. 3. The dual-parallel-buck converter was inversely derived from the dual-boost bridgeless power-factor correction (PFC) circuit.[14-17]

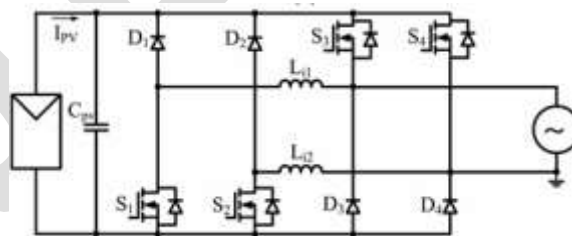


fig.3 Single phase transformerless PV dual-paralleled buck inverters.

The dual-paralleled buck inverter eliminates the problem of high conduction losses in the H5 and H6 inverter topologies because there are only two active switches in series with the current path during active phases. The main issue of this topology is that the grid is directly connected by two active switches S3 and S4, which may cause a grid short-circuit problem, reducing the reliability of the topology. A dead time of 500 μ s between the line-frequency switches S3 and S4 at the zero-crossing instants needed to be added to avoid grid shoot-through. This adjustment to improve the system reliability comes at the cost of high zero-crossing distortion for the output grid current one key issue for a high efficiency and reliability transformerless PV inverter is that in order to achieve high efficiency over a wide load range it is necessary to utilize MOSFETs for all switching devices. Another key issue is that the inverter should not have any shoot-through issues for higher reliability. [18-22]

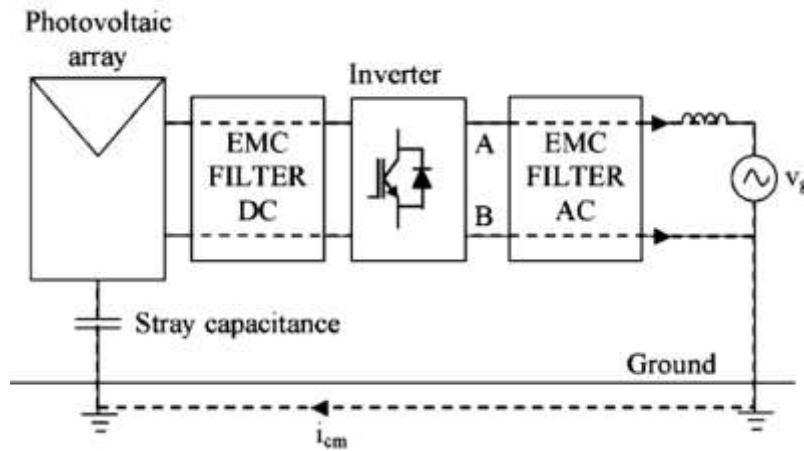


Fig.4 Common-mode currents in a transformerless conversion stage

In order to address these two key issues, a new inverter topology is proposed for single-phase transformerless PV grid-connected systems in this paper. The proposed converter utilizes two split ac-coupled inductors that operate separately for positive and negative half grid cycles. This eliminates the shoot-through issue that is encountered by traditional voltage source inverters, leading to enhanced system reliability. Dead time is not required at both the high-frequency pulse width modulation switching commutation and the grid zero crossing instants, improving the quality of the output ac-current and increasing the converter efficiency.

This paper is organized as section I is about the literature survey on transformerless PV inverter, sections II is presented about proposed topology with Sine PWM its principle of operation, section III is about common voltage analysis of proposed system, section IV matlab implementation of the proposed system with sine PWM and Phase Disposition technique. Comparison of two techniques for THD of output voltages with reduced leakage current is shown.

2. The Proposed Topology and Operational Analysis.

The proposed topology is shown in fig.5. Circuit diagram of the proposed transformerless PV inverter, which is composed of six MOSFETs switches (S1–S6), six diodes (D1–D6), and two split ac-coupled inductors $L1$ and $L2$. The diodes D1–D4 performs voltage clamping functions for active switches S1–S4. The ac-side switch pairs are composed of S5, D5 and S6, D6, respectively, which provide unidirectional current flow branches during the freewheeling phases decoupling the grid from the PV array and minimizing the CM leakage current.

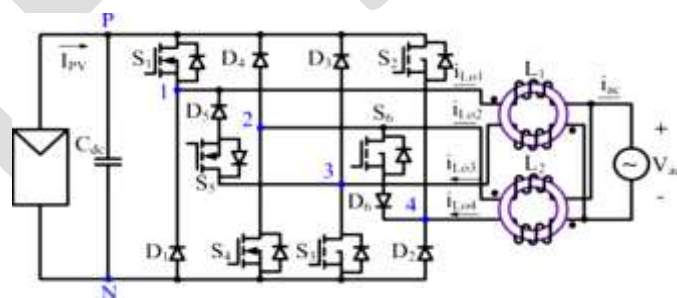


Fig.5 proposed high efficiency and reliability PV transform less inverter topology.

Compared to the HERIC topology the proposed inverter topology divides the ac side into two independent units for positive and negative half cycle. In addition to the high efficiency and low leakage current features, the proposed transformerless inverter avoids shoot-through enhancing the reliability of the inverter. The inherent structure of the proposed inverter does not lead itself to the reverse recovery issues for the main power switches and as such super junction MOSFETs can be utilized without any reliability or efficiency Penalties.

Fig.6 illustrates the PWM scheme for the proposed inverter. When the reference signal $V_{control}$ is higher than zero, MOSFETs S1 and S3 are switched simultaneously in the PWM mode and S5 is kept on as a polarity selection switch in the half grid cycle; the gating signals G2, G4, and G6 are low and S2, S4, and S6 are inactive. Similarly, if the reference signal $-V_{control}$ is higher than zero, MOSFETs S2 and S4 are switched simultaneously in the PWM mode and S6 is on as a polarity selection switch in the grid cycle; the gating signals G1, G3, and G5 are low and S1, S3, and S5 are inactive.

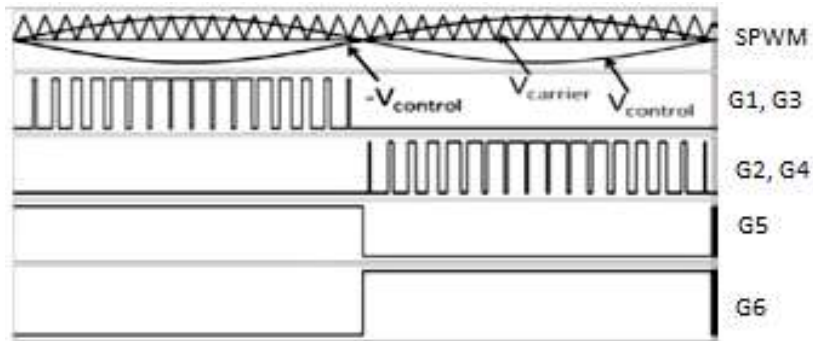


fig. 6 Phase disposition PWM signal used to control the system

Table 1 switching states and respective common mode voltages

S_1	S_2	S_3	S_4	S_5	S_6	V_{cm}	Sequence
pwm	off	off	pwm	on	off	$U_{dc}/2$	positive
off	off	off	off	off	off	$U_{dc}/2$	
off	pwm	pwm	off	of	on	$U_{dc}/2$	negative
off	off	off	off	off	off	$U_{dc}/2$	

Fig.7 shows the four operation stages of the proposed inverter within one grid cycle. In the positive half-line grid cycle, the high-frequency switches S_1 and S_3 are modulated by the sinusoidal reference signal $V_{control}$ while S_5 remains turned ON.

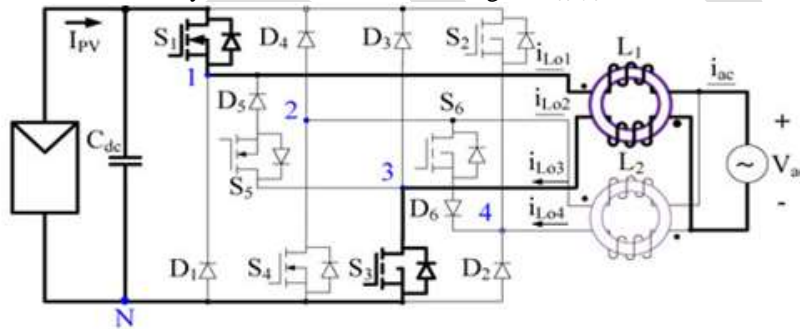


fig. 7 active stage of positive half-line cycle

When S_1 and S_3 are ON, diode D_5 is reverse-biased, the inductor currents of i_{Lo1} and i_{Lo3} are equally charged, and energy is transferred from the dc source to the grid.

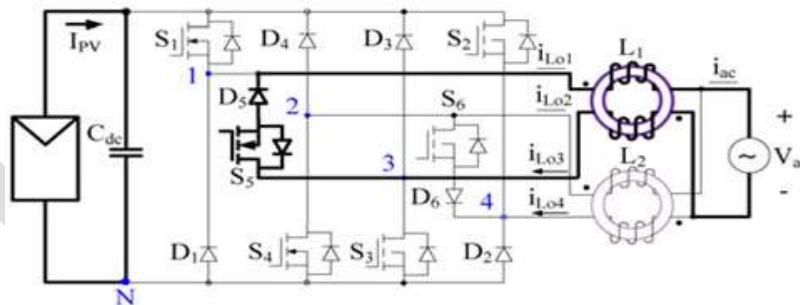


fig. 8 freewheeling stage of positive half-line cycle

When S_1 and S_3 are deactivated, the switch S_5 and diode D_5 provide the inductor current i_{L1} and i_{L3} a freewheeling path decoupling the PV panel from the grid to avoid the CM leakage current. Coupled-inductor L_2 is inactive in the positive half-line grid cycle.

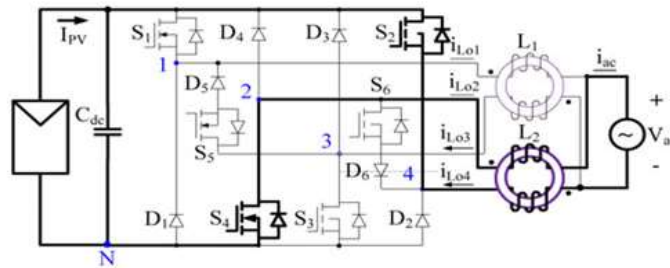


fig. 9 Active stage of negative half-line cycle

Similarly, in the negative half cycle, S2 and S4 are switched at high frequency and S6 remains ON. Freewheeling occurs through S6 and D6. When S2 and S4 are ON, diode D6 is reverse-biased, the inductor currents of i_{Lo2} and i_{Lo4} are equally charged, and energy is transferred from the dc source to the grid; when S2 and S4 are deactivated, the switch S6 and diode D6 provide the inductor current i_{L2} and i_{L4} a freewheeling path decoupling the PV panel from the grid to avoid the CM leakage current.

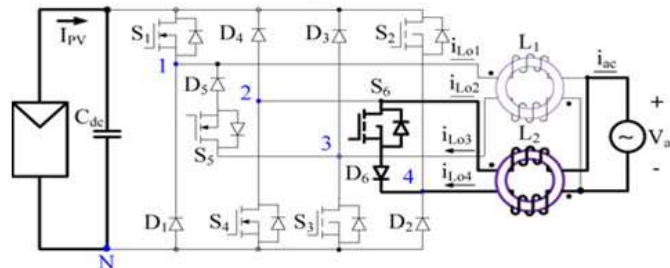


fig. 10 freewheeling stage of negative half-line cycle.

3. Ground Loop Leakage Current Analysis for the Proposed Transformerless Inverter

A galvanic connection between the ground of the grid and the PV array exists in transformerless grid-connected PV systems. Large ground leakage currents may appear due to the high stray capacitance between the PV array and the ground. In order to analyze the ground loop leakage current, Fig. 11 shows a model with the phase output points 1, 2, 3, and 4 modeled as controlled voltage sources connected to the negative terminal of the dc bus (N point).

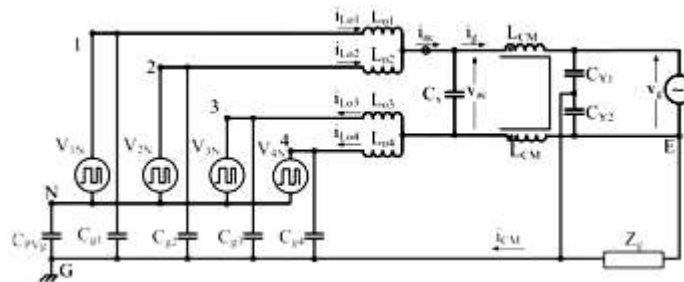


fig. 11 Simplified CM leakage current analysis model for positive half-line cycle

The value of the stray capacitances C_{g1} , C_{g2} , C_{g3} , and C_{g4} of MOSFETs is very low compared with that of $CPVg$, therefore the influence of these capacitors on the leakage current can be neglected. It is also noticed that the DM capacitor C_x does not affect the CM leakage current. Moreover, during the positive half-line cycle, switches S_2 , S_4 , and S_6 are kept deactivated; hence the controlled voltage sources V_{2N} and V_{4N} are equal to zero and can be removed. Consequently, a simplified CM leakage current model for the positive half-line cycle is derived as shown in Fig. 11

4. Matlab Verification of The Proposed Circuit

The figure 12 is the Matlab design of proposed system with unipolar pwm with the switching frequency of 20KHz. Sine PWM is used to generate the control signals to convert DC of supply into AC supply. The subsystem of Solar PV system is shown in figure 13.

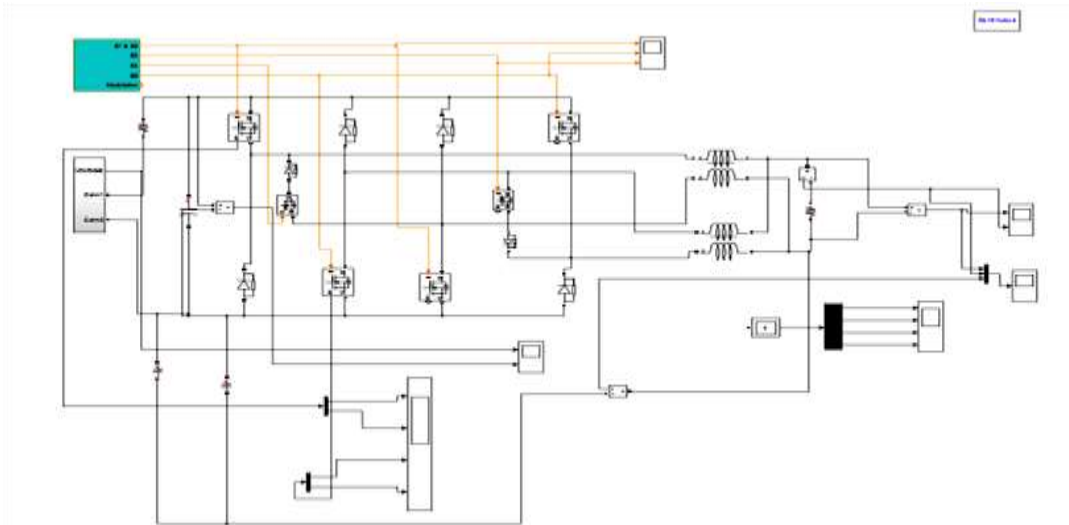


fig. 12 proposed circuit in Matlab

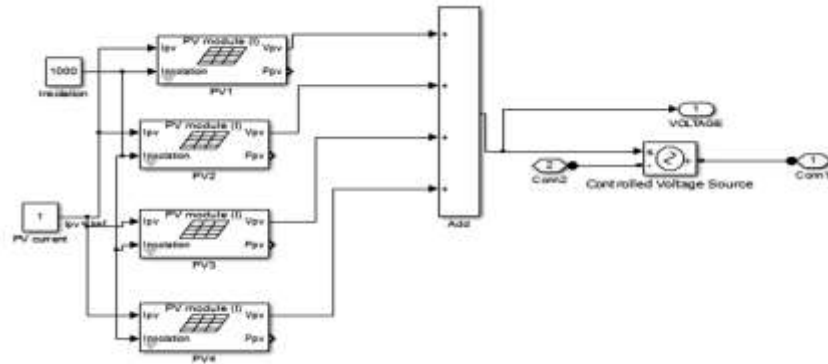


fig. 13 solar pv system design in Matlab

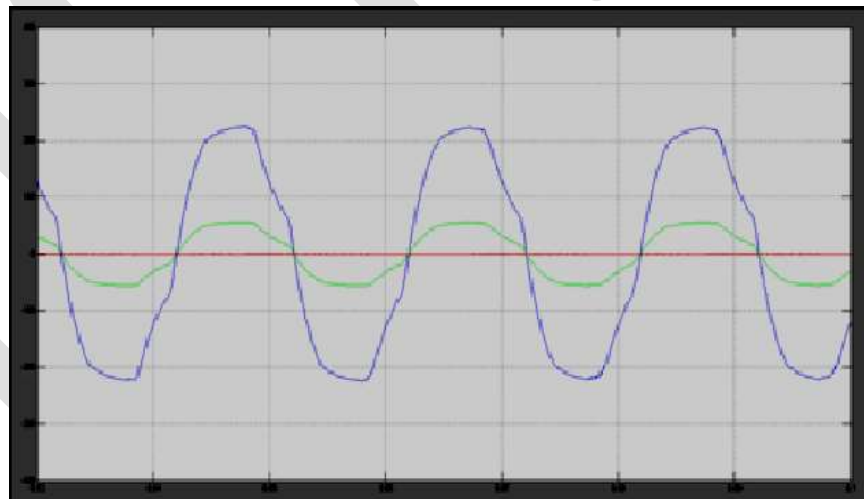


fig. 14 grid voltage and current

The inverter output voltage and current waveform is shown in figure 14 with output voltage of 230V , 50Hz and 4 amps of current is obtained as AC grid tie output. The green waveform is shown in figure represents the leakage currents due to common mode voltages.

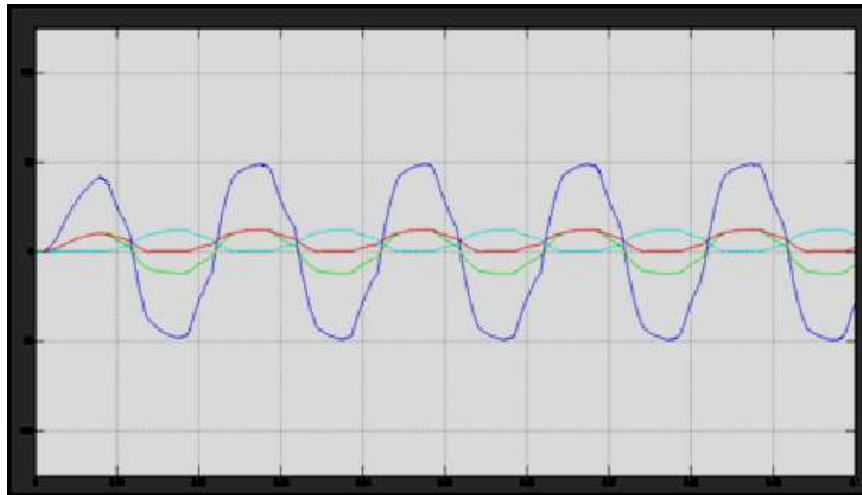


fig. 15 grid voltage, inductor currents of i_{Lo1} and i_{Lo2}

As shown in the proposed circuit the output of inverter is not directly connected to grid, two inductive filters are employed for positive half and negative half cycle of the output independently. The waveforms in figure 15 represent the currents through the inductors for positive and negative half of full cycle.

Figure 16 shows the closer image of the leakage current due to the common mode voltage. The figure 17 shows the individual currents that flow through the filter inductor during both half cycles.



fig. 16 Common mode leakage current

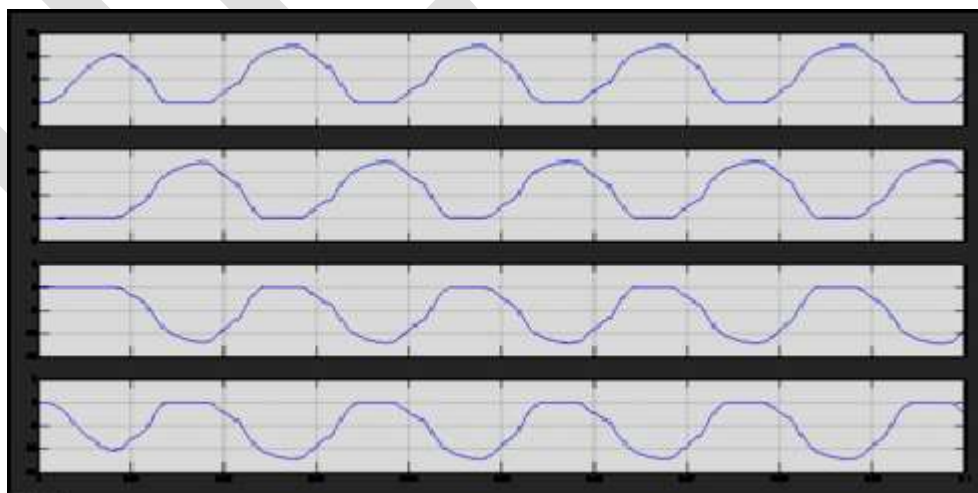


Fig. 17 inductor currents of i_{Lo1} , i_{Lo2} , i_{Lo3} and i_{Lo4}

The figure 18 shows the total Harmonic distortion of output voltage tied to grid while using sine PWM as the pulse generator, it is found that the THD is about 14.60%.

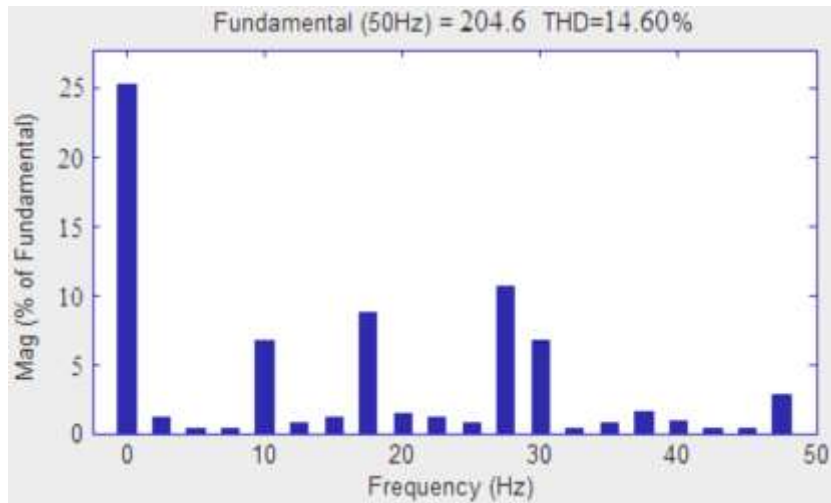


Fig. 18 THD of output voltage using SPWM technique

Phase opposition is the one of the efficient technique among the PD, POD, APOD, figure 19 shows the PD technique implemented by using Matlab for generating gate signals it is evident from figure 20 that the leakage current due to common mode voltage is became nearly to zero and the total harmonic distortion is reduced to 9.86%

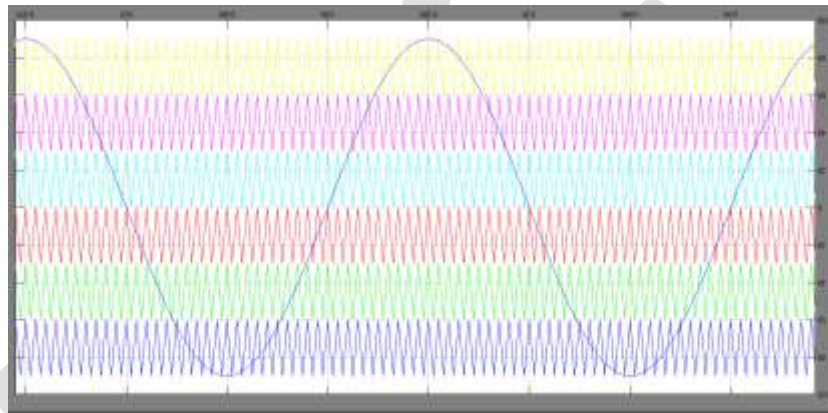


Fig. 19 Phase Disposition modulation applied to proposed system

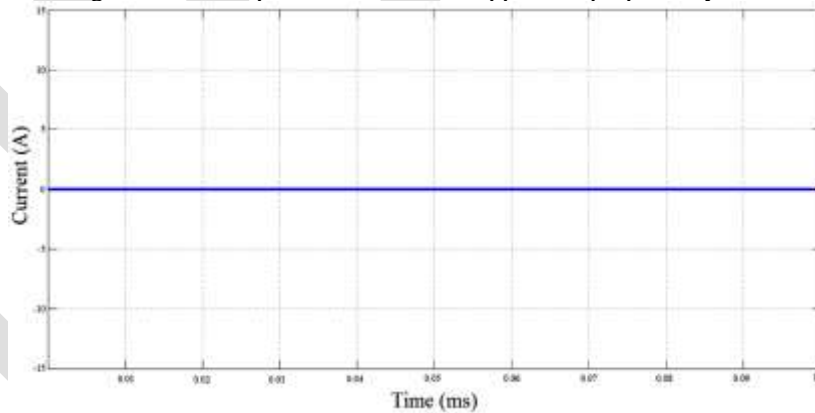


fig.20 Reduced Leakage currents when applying PD technique

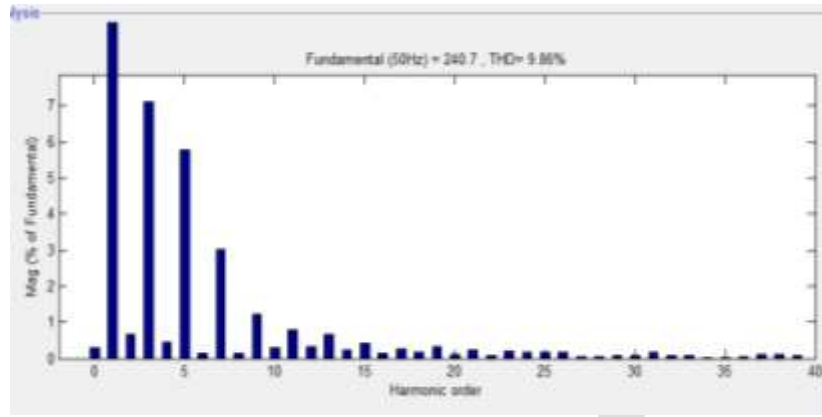


fig. 21 FFT analysis using PD technique

The figure 6 is the gate pulse generation for the proposed converter for 20KHZ operating frequency of converter. The figure 14 is the grid voltages and current at pcc. The Figure 17 gives grid voltage, inductor currents of i_{Lo1} and i_{Lo2} . The main of this project is reducing common mode currents is presented in figure 20. The figure 21 shows the THD of output voltage is about 9% shows that power quality is up to the mark. According to IEEE standard 5% of THD is acceptable limit.

5. Conclusion

A high reliability and efficiency inverter for transformerless solar PV grid-connected systems is presented in this paper using Matlab/Simulink model design. It is found that the leakage current present due to the effect of common mode voltage while using SPWM is reduced by using Phase Disposition technique. The main characteristics of the proposed transformerless inverter are observed are reduced shoot-through issue leads to greatly enhanced reliability, low ac output current distortion is achieved because dead time is not needed at PWM switching commutation instants in PD techniques and grid-cycle zero-crossing instants, low-ground loop CM leakage current are minimized to the standard, as a result of two additional unidirectional-current switches decoupling the PV array from the grid during the zero stages and higher switching frequency operation is allowed to reduce the output current ripple and the size of passive components while the inverter still maintains high efficiency. It is shown that the proposed transformerless PV grid tie inverter is efficient when using PD as PWM for controlling the switching operation with overall improved efficiency.

6. Future Scope

The asymmetry of the switch arrangements in less usage of the number of high frequency switches in order to reduce the losses and increase the efficiency of proposed system will be a good option.

Appendix

Parameters	Specifications
Input voltage	440V DC
Grid voltage/ Frequency	230V/50Hz
Rated Power	1000W
Switching Frequency	20KHz
Dc bus capacitor	470 μ F
Filter capacitor	4.7 μ F
Filter Inductors	2mH
Parasitic capacitors	750nF

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