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An Ultra-Wide-Band 2.66 - 3.75 GHz LNA in 0.18-µm CMOS Radio Frequency

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Abstract— An Ultra-Wide-Band Low Noise Amplifier is designed in this work. The designed LNA is of two stages that may be used in various applications in communication systems. The designed LNA is simulated by HSPICE in 0.18-µm CMOS Radio Frequency technology. This LNA has a gain of 20 dB which stays there from 3.06 GHz to 3.21 GHz and noise figure of 3.78 dB. HSPICE simulation shows the bandwidth as 1.09 GHz with a center frequency at 3.13 GHz. It consumes 13.4150 mW from a 1.8 V supply and has a 1 dB compression point of -16.2 dBm. Characterization of the designed LNA exhibits a high gain and considerably low noise figure with good impedance matching.

Keywords— LNA, CMOS_RF, Circuit and Systems, HSPICE, High Gain, S Parameters, Noise Figure & 1-dB compression point.

INTRODUCTION

Wireless communication system has been a very important and convenient way of communication for quite a long time. In recent years, in order to add some improvements in the system, the demand for high speed and high data rate wireless communication is increasing day by day. For IEEE 802.11b [1] and 802.11g standards [2] the operation frequency is 2.4 GHz with data rate 11 and 54 Mbps respectively [3]. At present, ultra-wide band (UWB) systems are emerging wireless technology capable of transmitting data over a wide frequency band for short ranges, which have the advantages of low power but at a superior data rate. The allocated band of UWB (IEEE 802.15.3a) is between 3.1 to 10.6 GHz [4]. For a wireless front-end, a wide-band low-noise amplifier (LNA) is critical in spite of the receiver architecture. The amplifier must meet quite a number of inflexible requirements such as - broadband input matching in order to minimize the return-loss, sufficient gain to suppress the noise of a mixer, low noise-figure (NF) to improve receiver sensitivity, low power consumption to increase battery-life and small die area to reduce the expense. There are several techniques available to UWB LNAs in literature [3]-[12]. However, there are certain limitations of these topologies. For example, the conventional distributed amplifier suffers from high power consumption [5]. Resistive feedback is a well-known wide-band technique used in wide-band amplifiers, but it is hard to satisfy the gain and noise requirements simultaneously. [6] Another solution is to embed the input network in a multi-section reactive network so that the overall input reactance is resonated over a wider bandwidth [4]. Although this filter type topology achieves wide-band matching, low power consumption and can suppress the high frequency variation depending on the technology; the insertion of filter adds noise at low frequency. On the contrary, NF grows hastily at higher frequency for CMOS technology. So to get desirable matching condition, inductor modeling in the filter must be accurate enough, or else, the bandwidth and flatness will be degraded.

So to overcome all these drawbacks, an UWB LNA is presented with the common gate in first stage and common source-common gate in second stage cascaded together. It needs only two inductors and a few resistances and the wide-band matching condition is achieved with low power consumption.

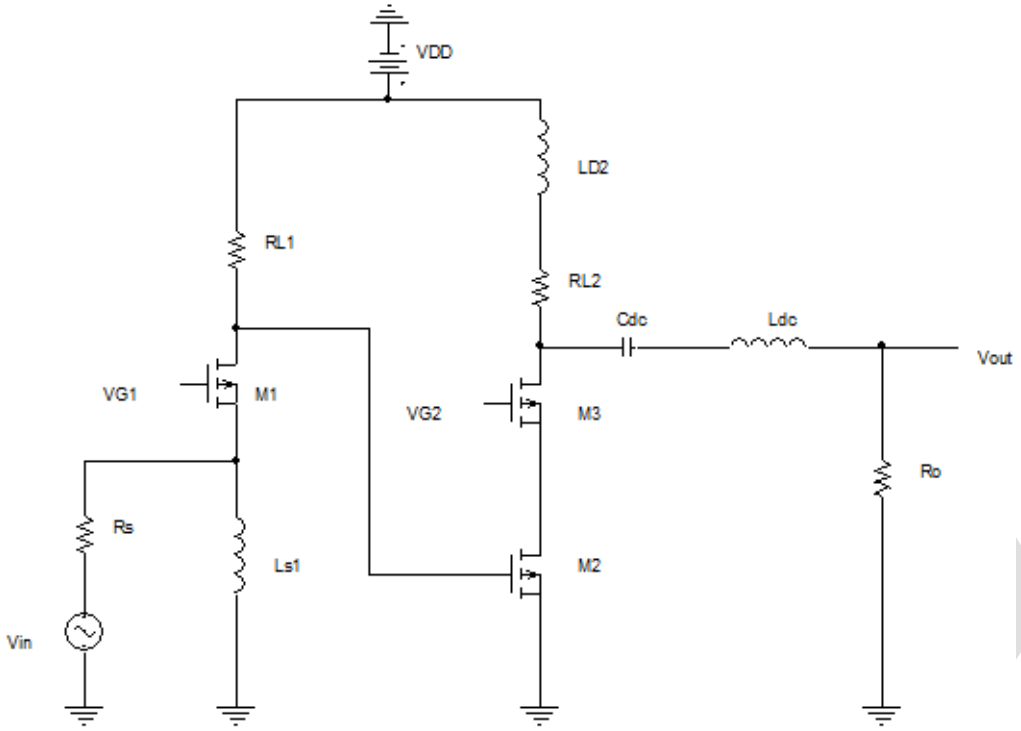

Figure 1 : Proposed UWB

CIRCUIT DESIGN

The designed circuit is two-staged consisting of a common-gate model and a common source-common gate configuration. It has been designed with three NMOS: M_1, M_2 and M_3. The input common-gate is there for providing wide-band input matching. It is the first stage of the model. It also provides power matching for the circuit. It offers a good input matching with the source. If we neglect the loading effect of the second stage and the parasitic resistance of input inductor (L_{S1}), the input impedance can be represented as follows:

$$Z_{in} = \frac{sL_{S1}}{1+(g_{m1}+sC_{gs1})sL_{S1}} \quad \text{.....(1)}$$

Here, g_{m1} is the transconductance and C_{gs1} is the gate to source capacitance of the transistor M_1. From the equation, it is clear that, there is a zero near DC which determines the low 3-dB frequency. The input inductor L_{S1}, at low frequency, gives very little impedance to ground. As a result, Z_{in} is dominated by L_{S1} and the value is negligible (almost zero). The chosen value of L_{S1} for this model is 8.3 nH. Even though the common-gate stage gives a wide-band input matching, it compensates with a narrow-band frequency response. The transfer function represented by the first stage is given as:

$$\frac{V_{D1}}{V_{in}} = \frac{(1+g_{m1}r_{o1})R_{L1}}{(1+\frac{R_S}{sL_{S1}}+sR_SC_{gs1})(r_{o1}+R_{L1})+(1+g_{m1}r_{o1})R_S} \quad \text{.....(2)}$$

While designing, size of M_1 is a special concern for proper input matching. Even the value of R_{L1} is critical here, since it determines the gain and gate bias for the first and second stages respectively. The best match was 280 Ω for fulfilling these entire requirements and it was accepted for the model.

A simple cascaded common source-common-gate is the second stage of the model. It offers high frequency gain and determines higher 3-dB bandwidth for the LNA. M_3, the cascode transistor, is used for better isolation, higher frequency response and higher gain. A series of peaking inductor L_{D2} of 10 nH is resonant with the total parasitic capacitance C_{D3} at the drain of M_3, which is around 10 GHz [9]. The transfer function for this stage is expressed as:

$$\frac{V_{D2}}{V_{D1}} = g_{m2} \times \left[(g_{m3} \bullet r_{o3} \bullet r_{o2}) // \left(\frac{R_{L2}\left[s\left(\frac{L_{D2}}{R_{L2}}\right)+1 \right]}{s^2 L_{D2} C_{D3} + sR_{L2} C_{D3} + 1} \right) \right] \quad \text{.....(3)}$$

In order to keep the parasitic capacitance lower, the cascode device M_3 is chosen to be smaller. The Q factor (quality factor) of the inductors for the LNA should be kept as high as possible in order to ensure high gain, narrow-band characteristics. However, in this design, the Q factor of L_{D2} is used for the flat gain of whole LNA. As a result an extra resistor R_{L2} of 50 Ω is added to reduce the Q factor.

For blocking any unwanted dc current, a series connection of a dc blocking capacitor of 180 fF (C_{dc}) and an inductor of 0.05 nH (L_{dc}) is used. A 100 kΩ resistor (R_o) is used in parallel for making the output open.

RESULT

The simulated result of the designed LNA is shown in the below section.

S-parameters are shown in fig. 4. S_{11} curve of our LNA remains always negative. From 1.39 GHz onward it remains under -10 dB point. Lowest value is -23.1 dB at 3.1 GHz and 4.15 GHz. At 3.13 GHz, which is the center frequency, value of S_{11} curve is -23 dB means perfect input matching. S_{11} should be below -10dB for perfect input matching.

S_{12} curve is also negative and below -47 dB at all times. S_{12} means input-output isolation. It becomes stable after 3 GHz and the value under stable condition is -51dB. At center frequency (3.13 GHz) this value is -52.2dB means high input-output isolation.

S_{21} means the gain of the amplifier. S_{21} curve becomes positive after 1.2 GHz and stays above 10 dB point from 2.04 GHz to 5.41 GHz. The curve reaches its highest peak, 20 dB and stays there from 3.06 GHz to 3.21 GHz. We succeeded to achieve considerably high gain, but we had to compromise the bandwidth which is 1.09 GHz starting from 2.66 GHz to 3.75 GHz.

Output matching parameter (S_{22}) curve is always negative. It is under -5 dB from 2.81 GHz to 3.4 GHz. Lowest values of the curve is -10 dB at 3.1 GHz. At center frequency it has a value of -9.85 dB.

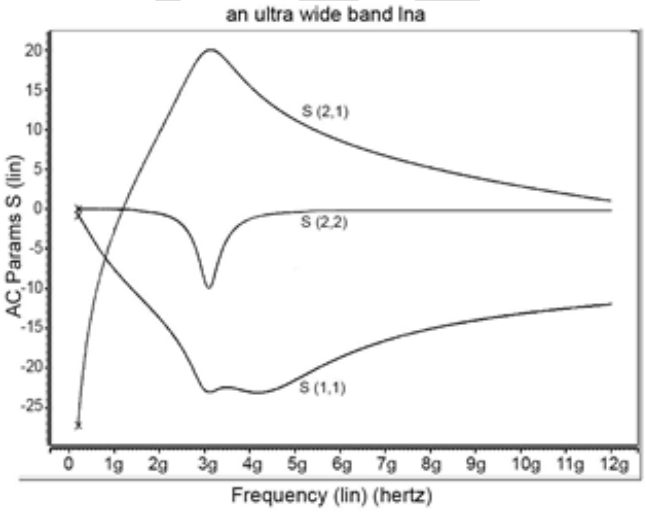

Figure 2: Simulation results for S11 , S12, S22

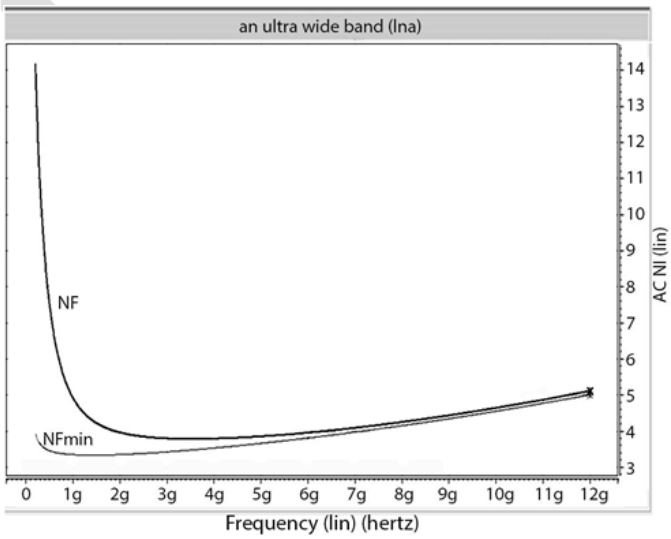

Figure 3: NF and NFmin

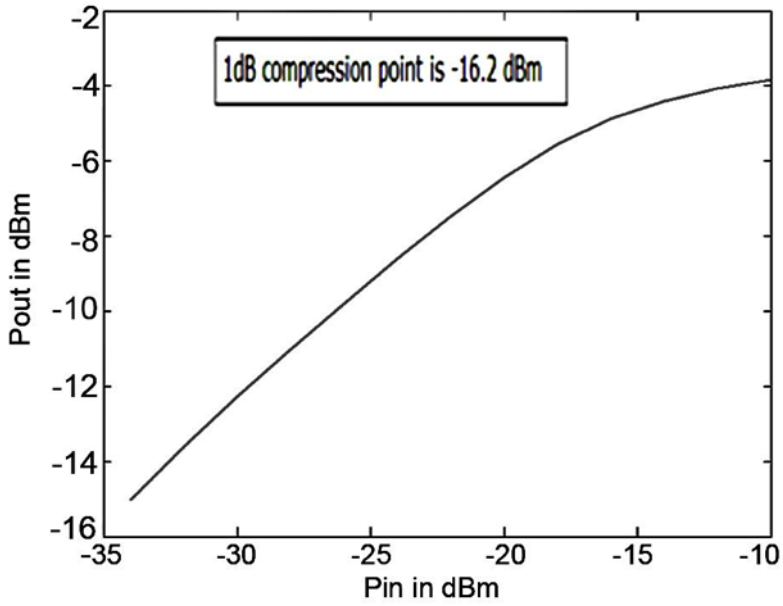

Figure 4: 1 dB compression point

Due to common-gate characteristics the NF does not rise in higher frequencies. The noise figure remains below 4 dB from 1.88 GHz to 6.43 GHz. Lowest value is 3.78 dB which starts from the center frequency (3.13 GHz) and stays constant till 3.97 GHz. Minimum noise figure is below 3.5 dB starting from 428 MHz to 3.7 GHz. Its lowest value is 3.13 dB at 1.4 GHz. At center frequency the value is 3.44dB.

Linearity of an amplifier is measured using 1-dB compression point. 1 dB compression point of the LNA is calculated to measure linearity of the circuit. The measured 1 dB compression point is -16.2 dBm. The power consumption can be considered reasonable which has a value of 13.4150 mW.

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CONCLUSION

An ultra-wide band (UWB) CMOS low noise amplifier (LNA) has been implemented in a 0.18 µm CMOS_RF process. The measured peak power gain is 20 dB and NF is 3.85 - 3.78 dB with 3 dB bandwidth of 2.66 - 3.75 GHz. Here input matching is below -17 dB between the bandwidth region and -23.1 dB at center frequency while the output matching is -10 dB at center frequency. The 1 dB compression point is -16.2 dBm. The designed LNA has the following advantages compared to other broad-band techniques: less design complexity, low noise, low power dissipation and high gain.

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