International Journal of Engineering Research and General Science Volume 5, Issue 3, May-June, 2017
ISSN 2091-2730

LOW POWER SQUARE AND CUBE ARCHITECTURES USING VEDIC SUTRAS

Parepalli Ramanammma[1], MALASHREE N [2]

[1]Assistant professor in Electronics Department,
New Horizon College of Engineering, VTU
Outer Ring road, Near Marthahalli
Bangalore – 560 103

[2] C BYREGOWDA INSTITUTE OF TECHNOLOGY
KOLAR
maturyrama@gmail.com

Abstract— In this paper low power square and cube architectures are proposed using Vedic sutras. Low power and less area square and cube architectures uses Dwandwa yoga Duplex combination properties of Urdhva Tiryagbhyam sutra and Anurupyena sutra of Vedic mathematics. Implementation results show a significant improvement in terms of area, power and delay. Proposed square and cube architectures can be used for high speed and low power applications. Synthesis and simulation is done using Cadence RTL simulator(180nm) Technology. Hardware implementation is done using Spartan6 Xilinx FPGA .Propagation delay of the proposed 8-bitsquare is 1.822ns and area consumed in terms of slicesis 22 and for 8-bit cube prorogation delay is 1.405ns.Total power estimation for square and cube are 0.0297mW and 0.194mW respectively.

Keywords— Vedic mathematics, Dwandwayoga, Anurupyena , Square, Cube, low power, less area.

INTRODUCTION

Vedic mathematics is the name given to ancient mathematical system which was rediscovered from the Vedas by Sri Bharati Krishna Tirthaji between 1911 and 1918. The most important feature of the Vedic mathematics system is its coherence. Instead of lengthy unrelated techniques the entire system is beautifully interrelated and unified. The general multiplication method can be easily reversed to allow one-line division also the simple squaring method can be reversed to get one-line square root. All these methods can be easily understood. The unifying quality of this system is its highlight, this makes mathematics easy and it will encourage innovation. In the past, conventional methods have been used for multiplication. Conventional methods have been highly time consuming.

Square and cube are frequently performed functions in most of the DSP systems. Square and cube are special cases of multiplication. Square and cube architectures forms the heart of the different DSP operations like Image Compression, Decoding, Demodulation, Adaptive Filtering, Least Mean Squaring etc., and also have numerous applications as mentioned in such as cryptography, computation of Euclidean distance among pixels for a graphics processor or in rectangular to polar conversions in several signal processing circuits where full precision results are not required. Traditionally, square and cube were performed using multiplier itself. As the applications evolved demand for the high speed processing increased, special attention was given for square and cube function.

In this paper algorithms and architectures used to design square and cube of a binary number is explored and to create a circuit using the Vedic Sutras. Often times square and cube are the most time-consuming operations in many of digital signal processing applications and computation can be reduced using the vedic sutras and the overall processor performance can be improved for many applications. Therefore, the goal is to create a square and cube architectures that is comparable in speed, power and area than a design using an standard multiplier. The motivation behind this work is to explore the design and implementation of Square and Cube architectures for low power.

This paper is organized as follows. Section 1 gives the overview of Vedic mathematics and Vedic mathematics sutras and sub-sutras. Section 2 briefs about square architecture. Section 3 details about cube architecture. Section 4 discusses about results and discussion and section 5 about the conclusion.

1. Overview of Vedic Mathematics

Vedic mathematics is the name given to the ancient system of mathematics. It was rediscovered by Jagadguru Swami Sri Bharati Krishna Tirthaji (1884-1960) between 1911 and 1918. He is a scholar of Sanskrit, mathematics, history and philosophy. The whole of Vedic mathematics is based on 16 Vedic sutras. These sutras are used in various mathematical fields. But only two out of these 16 sutras are popular for multiplication**.** It solves many mathematical problems that are related to geometry, arithmetic, quadratic equations, trigonometry, calculus and even factorization.

Vedic mathematics is not just a magic in the field of mathematics it is also very logical in obtaining the solutions to the mathematical problems. That's the reason it has be approved globally. The eminent characteristics of Vedic mathematics has lead it to across the Indian boundaries and become a very interesting topic of research in foreign countries. It solves many simple and complex mathematical problems especially arithmetic methods are very powerful yet very simple to use. This is very attractive method and provides us with algorithms that are very effective and can be used in many engineering branches such as signal processing and computing.

The wonder of Vedic mathematics is that it lowers the normal calculations in traditional mathematics to easy one because the Vedic formula depends on common principles in which our mind works. It consists of arithmetic rules which increases the speed. Vedic mathematics also gives some effectual algorithms which can be applied to different branches of engineering.

A. Vedic Mathematics Sutras

This list of sutra is taken from the book Vedic Mathematics which includes a full list of the 16 main sutras. The following are the 16 main sutras or formulae of Vedic math and their meaning in English.

1. Ekadhikena Purvena: One more than the previous
2. Nikhilam Navatascharamam Dastah: All from nine and last from ten
3. Urdhwa-tiryagbhyam: Criss-cross
4. Paravartya Yojayet: Transpose and adjust
5. Sunyam Samyasamuchchaye: When the samuchchaya is the same, the samuchchaya is zero, and i.e. it should be equated to zero.
6. (Anurupye) Sunyamanyat: If one is in ratio, the other one is zero.
7. Sankalana-vyavkalanabhyam: By addition and by subtraction
8. Puranpuranabhyam: By completion or non-completion
9. Chalana-Kalanabhyam: Differential
10. Yavdunam: Double
11. Vyastisamastih: Use the average
12. Sesanyankena Charmena: The remainders by the last digit Sopantyadyaymantyam: The ultimate & twice the penultimate
13. Ekanyunena Purven: One less than the previous Gunitasamuchachayah: The product of the sum of coefficients in the factors
14. Gunaksamuchchayah: When a quadratic expression is product of the binomials then its first differential is sum of the two factors

B. Vedic Mathematics Sub-Sutras

1. Anurupyena: Proportionately
2. Sisyate Sesasamjnah: Remainder remains constant
3. Adyamadyenantyamantyena: First by first and last by last
4. Kevalaih Saptakam Gunyat: In case of seven our multiplicand should be 143
5. Vestanam: Osculation
6. Yavdunam Tavdunam: Whatever the extent of its deficiency, lessen it still further to that very extent
7. Yavdunam Tavdunam Varganchya Yojayet: Whatever the extents of its deficiency lessen it still further to that very extent; and also set up the square of that deficiency.
8. Antyayordasakepi: Whose last digits together total 10 and whose previous part is exactly the same
9. Antyayoreva: Only the last terms
10. Samuchchyagunitah: The sum of the coefficients in the product
11. Lopanasthapanabhyam: By alternate elimination and retention
12. Vilokanam: By observation

13. Gunitsamuchchayah Samuchchayagunitah: The product of sum of the coefficients in the factors is equal to the sum of the coefficients in the product

2. Square Architecture

Square Architecture using dwandwa yoga property of urdhwa tiryagbhyam sutra . Yavadunam Sutra is used for Squaring , is limited to the number which are near the base 10,100 etc.,The "Ekadhikena Purvena Sutra" is used for Squaring, is limited to number which ends with digit 5 only. The other method "Dwandwa Yoga" or Duplex is used in two different senses. The first one is by squaring and the second one is by cross multiplication. It is used in both the senses (a2 , b2 and 2ab).

In order to calculate the square of a number "Duplex" D property of Urdhva Tiryagbhyam is used. In the Duplex, take twice the product of the outermost pair, and then add twice the product of the next outermost pair, and so on till no pairs are left. When there are odd number of bits in the original sequence there is one bit left by itself in the middle, and this enters as its square. Thus for 987654321

D= 2 *(9* 1)+2 * (8 * 2)+2*(7 * 3)+ 2 *(6 * 4)+5 * 5=165.

Further, the Duplex can be explained as follows

1. For a 1 bit number D is its square.
2. For a 2 bit number D is twice their product
3. For a 3 bit number D is twice the product of the outer pair + the square of the middle bit.
4. For a 4 bit number D is twice the product of the outer pair + twice the product of the inner pair.

Thus

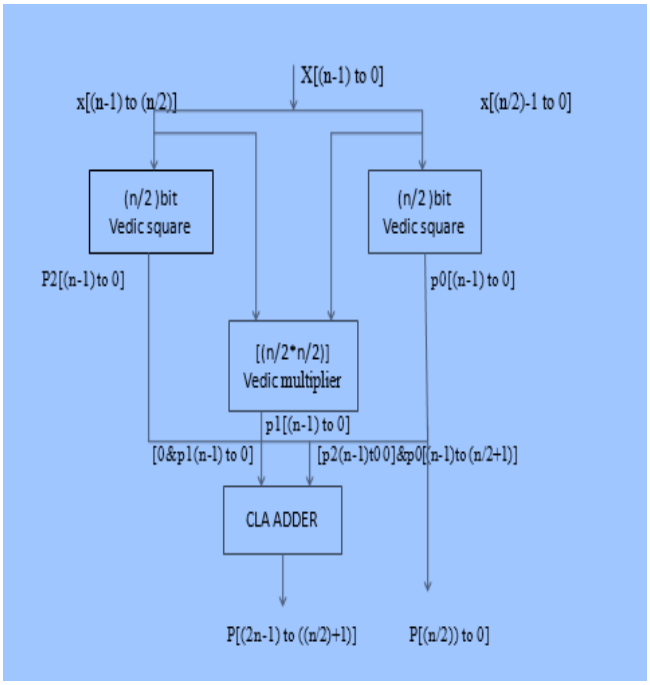
D (1) = 1 * 1;

D (11) =2 * 1 * 1;

D (101) =2 * 1 * 1+0 * 0;

D (1011) =2 * 1 * 1+2 * 1 * 0;

The vedic square has many advantages over the vedic multiplier. The block diagram of vedic square is as shown below:



As shown in the block diagram first [((n/2)-1) to 0]-bit of final product is obtained by directly taking the [((n/2)-1) to 0]-bit result of first squarer module (Least Significant Bit (LSB)-bits squarer). The result of the second squarer (Most Significant Bit (MSB)- bits squarer) is concatenated with remaining bits of first squarer and it is added with multiplier module results by concatenating ((n/2)-1) zeros at the MSB side and one zero at the LSB side.The sum produced by CLA adder gives the remaining [(2n-1) to (n/2)]-bit product. In optimization two due to reduced PPs andusing (n+(n/2)-1)-bit adder there is considerable amount of reduction in power consumption and propagation delay.

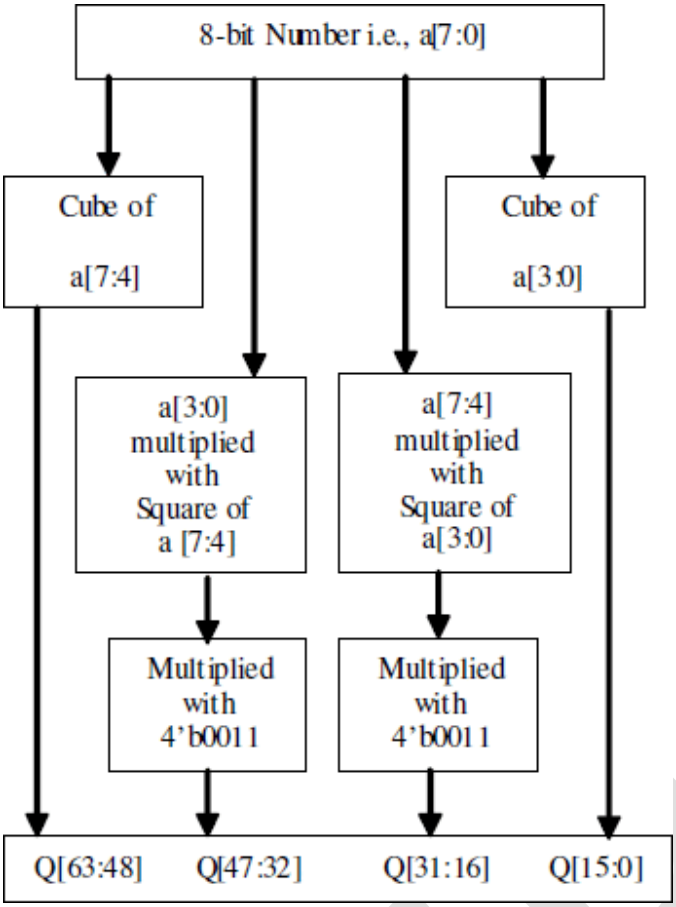
3. Cube Architecture

Cubing plays a vital role in secure communication systems, Signal Processing Applications, Finite Field Arithmetic etc. As the radix of the number used for cubing increases the process gets complicated which in turn increases the delay and power consumption**.**

In this paper the Anurupya Vedic sutra is used for cubing operations. The cubing operation is one of the most important operations in arithmetic process and it is found to be complicated, as we go for higher radix numbers. Cubing operation can be performed using ordinary multipliers, which are scalable but they have a larger delay Structure based array implementations are faster but scalability increases design complexity as well as expense.

Moreover, multipliers occupy large area, have long latency and consume considerable power. Therefore, multipliers which offer either of the following design targets-scalability, reconfigurability, high speed, low power consumption, regularity of layout and less area or even a combination of some of these features are welcomed. The Anurupya sutra of Vedic mathematics provides an efficient way of constructing a straight cubing system without using conventional multiplication methods.

The proposed cube is based on the Anurupya Sutra of Vedic Mathematics which states “If you start with the cube of the first digit and take the next three numbers(in the top row) in a Geometrical Proportion (in the ratio of the original digits themselves) you will find that the 4th figure (on the right end) is just the cube of the second digit”. The algebraic explanation is as follows: If a and b are two digits, then according to Anurupya Sutra., which is exactly equal to (a+b)3. This sutra has been utilized in this work to find the cube of a number. The number M of N bits having its cube to be calculated is divided in two partitions of N/2 bits, say a and b, and then the Anurupya Sutra is applied to find the cube of the number. a3 and b3 are to be calculated in the final computation of (a+b)3. The intermediate a3 and b3 can be calculated by recursively applying Anurupya sutra. The below is the block diagram of cube architecture.



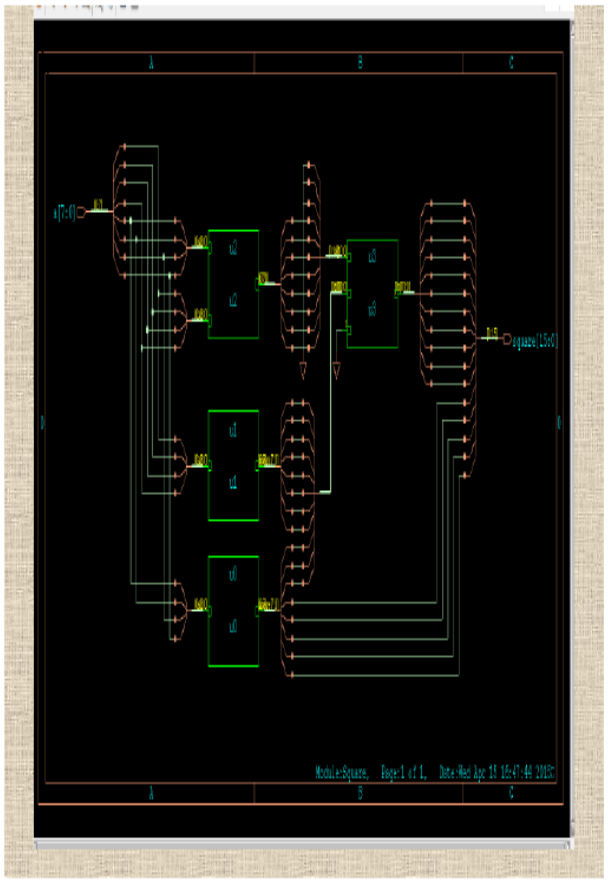
The first row can also be expressed as writing the numbers from the cube of the first digit to the cube of the second digit such that the numbers in between form the same ratio with respect to each other. In other words, the numbers in the first row are in geometric progression from the cube of the first digit to the cube of the second digit. In fact the constant ratio of the geometric progression is the same as the ratio between the first and second digits of the number to be cubed.

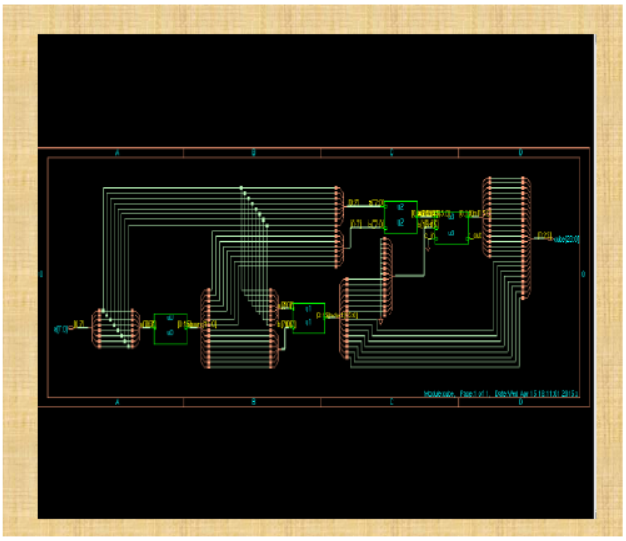
4. RESULTS AND DISCUSSIONS

In this work, 8-bit squaring and cube architectures are implemented in Verilog HDL . Logic synthesis and simulation are done in cadence RTL simulator tool 180nm technology . Hardware implementation is done using spartan 6 xilinx FPGA device. The results are displayed in Table for square and cube architecture of 8-bit size. These Table show the difference in delay, area utilization and low power estimation.

SYNTHESIS RESULTS:

8-BIT VEDIC SQUARE





8 bit vedic cube

Table:

Parameter	Delay (ns)	Area (slices)	Power (mW)
Square	**1.82**	**22**	**0.02**
Cube	**4.20**	**58**	**0.19**

5. CONCLUSION

Due to its regular and parallel structure it can be concluded that Vedic Square and cube are faster than conventional square and cube. Due to factors of timing efficiency, speed, low power and less area the proposed Vedic square and cube can be implemented in Arithmetic and Logical Units replacing the traditional square and cube circuits. It is demonstrated that this design is quite efficient in terms of area, speed & low power. Squaring of binary numbers of bit size other than powers of 2 can also be realized easily. For example, squaring of a 24-bit binary number can be found by using 32- bit squaring circuit with 8 MSBs (of inputs) as zero. The idea proposed here may set path for future research in this direction. Future scope of research is to reduce area requirements.

REFERENCES:

[1] Swami Bharati Krisna Tirthaji, "Vedic Mathematics," Motilal Banarsidass Publishers, Delhi, 1965.
[2] Himanshu Thapliyal, S. Kotiyal and M.B. Srinivas, "Design and Analysis of a Novel Parallel Square and Cube Architecture Based on Ancient Indian Vedic Mathematics", Proceedings on 48th IIEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005).
[3] Kabiraj Sethi, Rutuparna Panada, "An Improved Squaring Circuit for Binary Numbers" , International Journal of Advanced Computer Science and Applications, Vol. 3, No. 2, 2012.
[4] Implementation of high performance binary squarer circuit "by pradeep M C, 05, Article 09410, September 2014.
[5] A Novel Time and Energy Efficient Cubing Circuit using Vedic Mathematics for Finite Field Arithmetic Ramalatha M, Thanushkodi K, Deena Dayalan K, Dharani P.
[6] H. Thapliyal and M. B. Srinivas, "High Speed Efficient N × N Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Enformatika Trans., vol. 2, pp.225-228, Dec. 2004.
[7] Y.Yu Fengqi and A. N.Willson,"Multirate digital square architectures," in Proc. 8th IEEE Int. Conf. on Electronics, Circuits and Systems (ICECS 2001), Malta, Sept. 2–5, 2001, pp.177–180.
[8] P. D. Chidgupkar and M. T. Karad, "The Implementation of Vedic Algorithms in Digital Signal Processing", Global J. of Engg. Edu., vol. 8, no. 2, pp. 153–158, 2004.
[9] H. Thapliyal and M. B. Srinivas, "High Speed Efficient N × N Bit Parallel Hierarchical Overlay Multiplier Architecture Based on Ancient Indian Vedic Mathematics", Enformatika Trans., vol. 2, pp. 225-228, Dec. 2004.
[10] J.Bhasker, "Verilog HDL Primer" BSP Publishers, 2003.
[11] Himanshu Thapliyal, S. Kotiyal and M.B. Srinivas, "Design and Analysis of a Novel Parallel Square and Cube Architecture Based on Ancient Indian Vedic Mathematics", Proceedings on 48th IIEEE International Midwest Symposium on Circuits and Systems (MWSCAS 2005)
[12] Himanshu Thapliyal and Hamid R. Arabania, "A Time- Area – Power Efficient Multiplier and Square Architecture Based on Ancient Indian Vedic Mathematics", proceedings on VLSI04, Las Vegas, U.S.A, June 2004
[13] Kabiraj Sethi, Rutuparna Panada, "An Improved Squaring Circuit for Binary Numbers" , International Journal of Advanced

Computer Science and Applications, Vol. 3, No. 2, 2012.

[14] Vaijyanath Kunchigi, Linganagouda Kulkarni and Subhash Kulkarni 32-BIT MAC UNIT DESIGN USING VEDIC MULTIPLIER – published at: "International Journal of Scientific and Research Publications (IJSRP), Volume 3, Issue2, Feburary 2013 Edition".