International Journal of Engineering Research and General Science Volume 6, Issue 4, July-August, 2018
ISSN 2091-2730

INTERLEAVED THREE-PHASE THREE-LEVEL AC-DC SINGLE-STAGE PFC CONVERTER

G. Bindu[1],Mrs. K. S. L. Lavanya [2]
[1]PG Scholar, EEE, lakireddy Balireddy College of Engineering,himabindu0105@gmail.com
[2] Assistant Professor, EEE, lakireddy Balireddy College of Engineering , srilakshmilavanya@gmail.com

ABSTRACT

A new interleaved single-stage three- phase ac-dc power factor correction PFC converter is planned in this paper. The planned converter is based on the soft switching control procedure i.e; zero voltage switching with the intention that some of the switches turned on softly. The planned converter that uses phase-shift pulse width modulation (PWM) is offered at light-load conditions to get better the converters efficiency. Because of its interleaved structure the proposed converter can produce input current lacking harmonics. In this planned paper, the procedure of original converter is clarified and its features are discuss and its function is corresponding to another model converter.

Keywords: AC-DC power supplies, phase-shift pulse width modulation (PWM), three-level converters, three-phase converters, single-stage converters.

1.INTRODUCTION

Power factor correction (PFC) needs ac-dc power supplies to obey with harmonic standards IEC 1000-3-2[1].Some of the pulse width modulation (PWM) techniques are given in below points.

To get the input current more sine wave the earlier methods that uses the filters i.e; the inductors and capacitors to filter out low-frequency input current harmonics while these converters implemented with power factor correction should be expensive and simple so that these converters are also heavy and bulky. So that these applications are used limitedly. Some of the two-stage converters use a pre regulator to get the input current sine wave and the dc-dc converter will produce the desired output voltage and have to control the intermediate dc bus voltage. This converters require two separate switch-mode converters so that overall ac-dc converters price and complication is improved. The dc-dc conversion in a single power converter that can be corrected by a power factor in a single-stage power factor correction (SSPFC) converters. Depending upon two-stage converters, these converters are simple and cheap. some of the single-phase converters(5-7) and the thrre-phase converters(7-18) are planned in this prose.

In the earlier planned papers three-phase single-stage ac-dc converter have the drawbacks that can be classified as follows.

1. Here we are implementing the three separate ac-dc boost converter modules[2], [7]-[9] that can increases the cost and introduce the problems related to the synchronization of all ac-dc boost converter modules.
2. The converters used is resonant-type converters that can need the variable switching frequency control methods to operate so that the converter must be controlled by using very sophisticated techniques and/or nonstandard techniques[3]-[6].
3. Here the ac-dc converter results the output current should be discontinuous and it results a very high output ripple so that the high rating secondary diodes with peak current and large output capacitors are needed to filter out the ripples[7]-[12], [14].
4. The three-phase ac-dc converters can be exposed to very high voltages, because the three-phase ac-dc converters can be implemented with bulk capacitors and switches with very high-voltage ratings [11]-[13].
5. Three-phase converter need to have a large-input filter, that can filter out the large input current ripples as this current is discontinuous with high peaks.
6. The converter planned in [18] mitigates the above following drawbacks. Even though the proposed converter in [18] [20] these papers were an advance more than earlier planned three-phase single-stage converters, then also these converters require to operate at light-load conditions that have a irregular output inductor current to keep the dc link

capacitor below 450v and these converters will require to operate with input current that which is discontinuous which results high component stress and for the reason that of large amount of ripples in the input there is need to have a considerable filtering in the input.

The paper that which is proposed in [21] is shown in figure 1, is a new three-phase single-stage PFC AC-DC converter which is having the interleaved construction in the modern power electronics this interleaved construction is more popular[22]-[23].

The converter proposed in the paper [21] has some of the disadvantage, that the center tapped transformer is very costly to construct, which results same voltage lying on every half of the secondary windings. And the output is half of the secondary voltage, as each and every diode utilizes simply one half of the transformers secondary voltage. So that the output voltage of secondary winding of the transformer is double the times of the magnetizing voltage i.e; $2v_m$ when compared to the input power supply. Hence from the above discussion it is very clear that the cost of the circuit become expensive.

In the planned paper, interleaved three-phase three-level AC-DC single stage PFC converter with standard phase-shifted pulse width modulation (PWM) is explained and procedure of original converter is clarified and its features are discuss and its function is corresponding to another model converter.

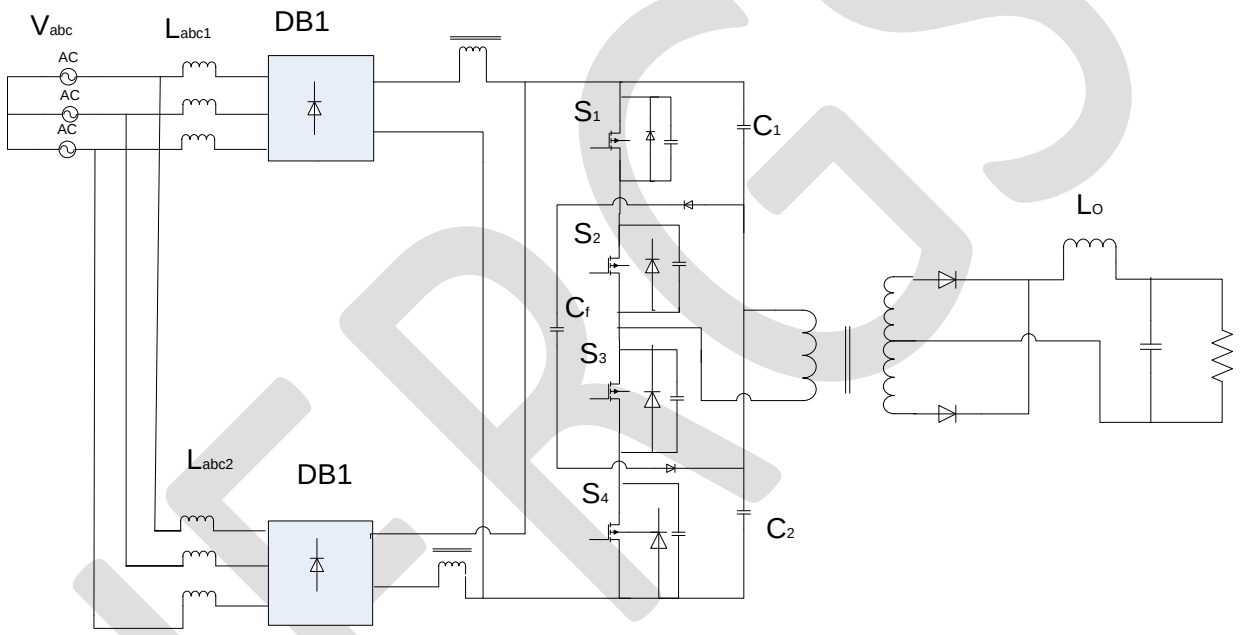


Fig. 1. Interleaved single-stage three-level converter**.**

2. CIRCUIT DESCRIPTION

The basic diagram of proposed converter is shown in figure . The basic drawing is related to that of three-phase single-stage PFC AC-DC converter as presented in the earlier paper[21]. Here v_{abc} is the three-phase ac supply voltage. The three input inductors L_{abc1} are coupled to each other to a diode bridge rectifier $DB_1$and the other three input inductors L_{abc2} are connected to each other to a diode bridge rectifier DB_2. The proposed converter can be taken from the converter transformer of additional windings that can be capable to work like a magnetic switches that can cancels the output voltage of dc-link capacitor after that this output voltage of diode bridge is zip. Here four power MOSFETs are connected with the aim of which can be termed as switches S_1,S_2,S_3,S_4 and D_1, D_2,D_3, D_4 can be reffered as the full bridge rectifier.

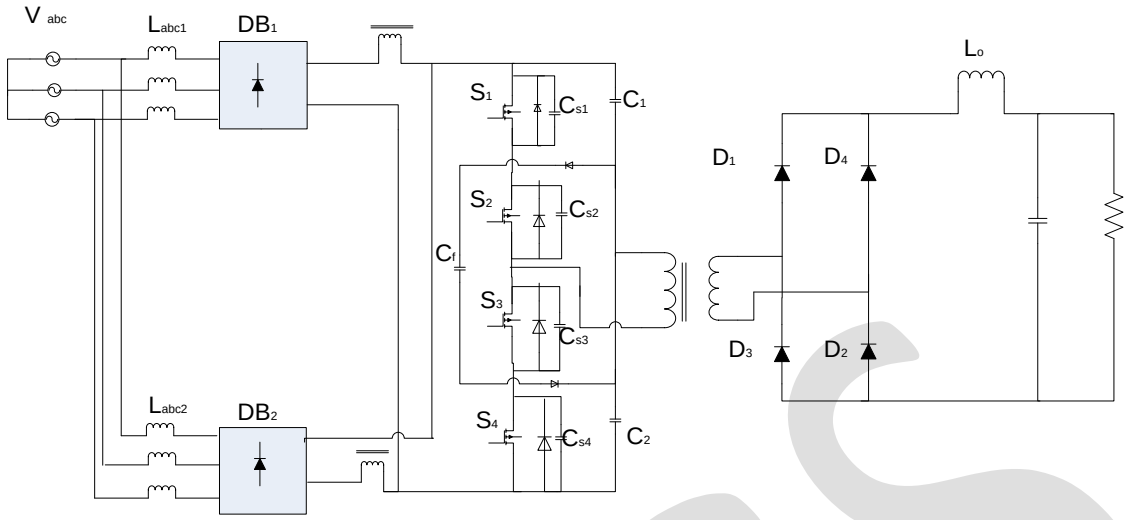


Fig. 2. Proposed topology of Three-phase three-level converter**.**

3.OPERATION OF THE CONVERTER

Mode 1($t_o \leq t \leq t_1$): In this mode of operation the switches s_1 and s_2 are turned ON. During this interval the flying capacitor C_f and both the dc bus capacitors C_1 and C_2 are charged to half of the dc bus voltage, and then the dc bus capacitor C_1 flows to the load output. Because of magnetic coupling, voltage appears from corner to corner the additional windings is equal to dc bus voltage and then this voltage totally cancels the dc bus voltage at the capacitor; then the output of the diode bridge voltage is zip so that the inductor currents iL_{a1} , iL_{b1} , iL_{C1} at the input will increase. And at the secondary side of the transformer the diodes D_1 and D_2 starts conducting at the same time to flow the energy into load.

Mode 2($t_1 \leq t \leq t_2$): In this mode of operation the switch s_1 is in turned off condition and the switch s_2 will remains ON. In the earlier mode of operation power stored in the input additional inductor starts being transferred into the dc bus capacitors then this energy will transfers into the capacitor c_{s1} charges and capacitor c_{s4} discharges through the flying capacitor c_f until the voltage across c_{s4}, the capacitance output of s_4 is clamped to zero. When switch s_4 turns ON with zero voltage switching then this mode ends, from the previous mode of operation the diodes are still conducting in the secondary side of the transformer.

Mode 3($t_2 \leq t \leq t_3$): In this mode of operation still the switch s_1 is in turned off condition and the switch s_2 will remains ON. In the earlier mode of operation stored power in the additional inductor input L_1 transfers to the dc bus capacitors. In the additional winding 1 the voltage that can be appeared is zip. The main transformer of the primary current can be passed through the diode D_1 and switch s_2. With the help of converters load side section, the output inductor current free wheels the main transformers secondary side, then the output inductor voltage is equal to $-V_L$.

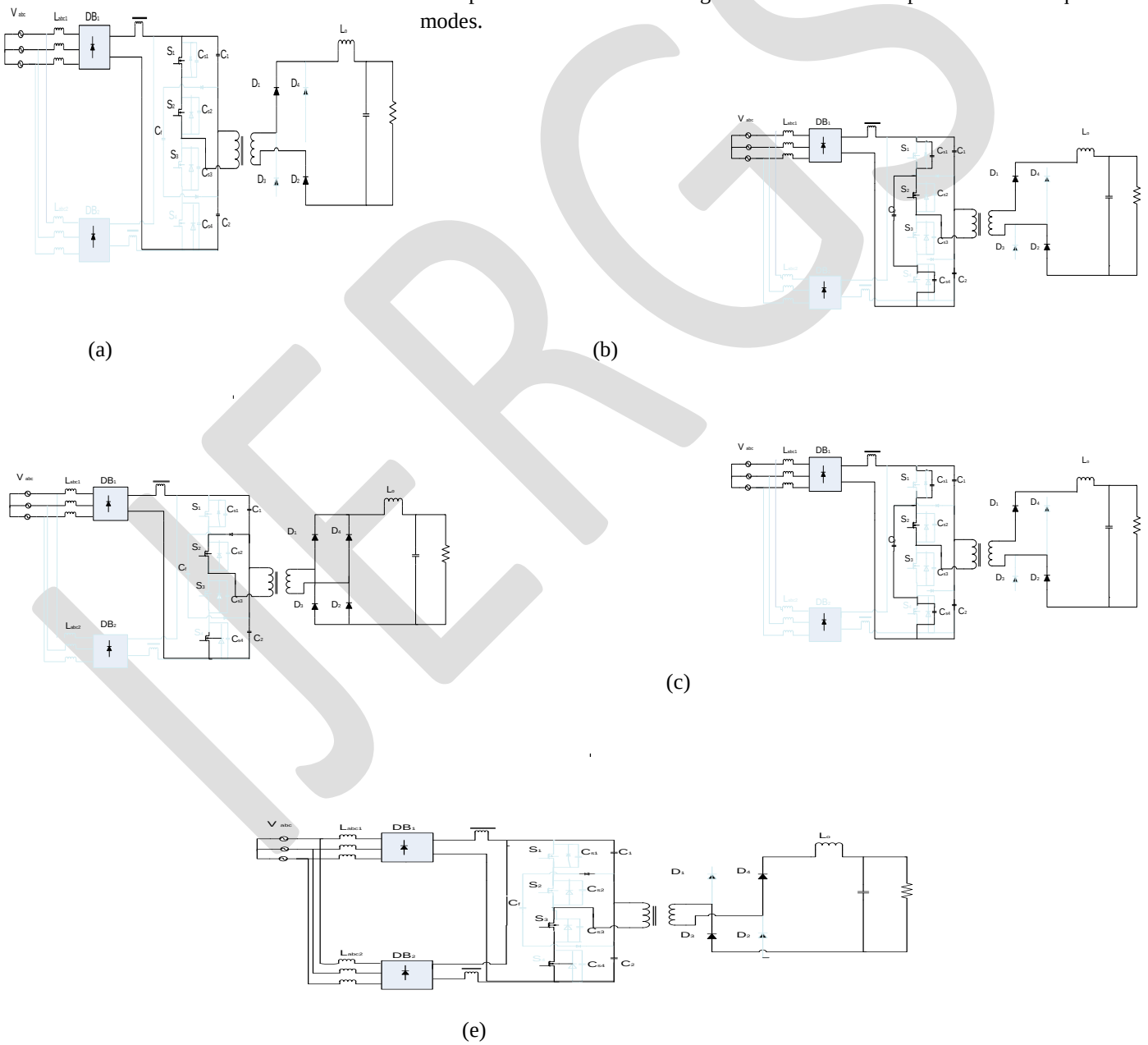
Mode 4($t_3 \leq t \leq t_4$): In this mode of operation both the switches S_1 and S_2 are turned OFF. The power stored in the additional inductor input L_1 is still transferred to the dc bus capacitors. The main transformers prime current can be discharge throughout the remains diode of switch S_3 due to the enough power in the outflow inductance. With respect to the capacitor C_2 this prime current will be charged through the body diodes of switches S_3 and S_4. Whenever the switch S_3 will be switched ON then this mode ends. And the diodes D_3 D_4 are conducting at the same time in the secondary side of the transformer to flow the energy to load.

Mode 5($t_4 \leq t \leq t_5$): In this mode of operation both the switches S_3 and S_4 are turned ON and the power flows from capacitor C_2 to the load and the voltage results from corner to corner additional winding is same to that of dc bus voltage however by means of reverse polarity that can nullify the dc bus voltage. The voltage at boost inductors L_2 becomes only the rectified supply voltage of every phase and the current flowing through the each inductor increases. The energy stored in the inductor L_1 is completely discharges into the dc link capacitor then this mode will be ended. For the remaining switching cycle, the planned converter under goes S_4 through Modes 6-

10, which are equal to the Modes1-5 as an alternative of S_1 and S_2 the switches S_3 and S_4 are ON and the diode bridge DB_2 starts conducting the current as an alternative of DB_1.

As there are two sets of inductors, there will be two sets of input inductor currents which will operate in discontinuous mode. As we know that the input is sum of i_{l1} and i_{l2} this current will be produced by two sets of inductors. In order to make the current flow to converters proper selection of $L_{a1} = L_{b1} = L_{c1}$ and $L_{a2} = L_{b2} = L_{c2}$ should be made in order to obtain the currents i_{la1} and i_{la2} to overlap each other. The currents i_{l1} and i_{l2} are produced by 180 phase difference in which one of the currents has obtained by impressing the transformer primary with a positive voltage and the other by the negative voltage.

In order to generate the gating signals a standard phase shift PWM IC is used which was S_2 S_2 implemented in this paper. During one mode of operation the switches S_2 and S_3 are not acceptable to be ON at the same time as well. When the switches S_1 S_2 or S_3 S_4 are ON then the converter will be under energy-transfer mode. Similarly when S_1 S_3 or S_2 S_4 are ON then the operation will be under freewheeling mode. In one switching cycle an alternating energy-transfer and freewheeling modes takes place in a standard two-level phase shift PWM full bridge converter that corresponds to same sequence or modes.



(a) (b) (c) (d) (e)

Fig. 3. Operating stages of circuit for time intervals from (a) [t_0-t_1] to (e) [t_4-t_5].

4. Design considerations

To design the planned paper the following considerations that should be taken into the account are discussed in this paper. The key parameters and its values in the planned converter are transformer turns ratio, output inductor, and input inductor are explained.

A. Transformer Turns Ratio N

The dc bus voltage at primary side is effected by the value of number of turns ratio (N). In order to discharge the bus capacitors, the turns ratio determines the load current that was presented at the primary side of the transformer. The conduction losses will be high when the number of turns ratio is low which indicates the current at primary side will be too great. And the conduction losses will be low when the number of turns ratio is high which indicates the current at primary side will be too low. In this case the converter can produce that can need the output voltage and can operate with discontinuous input and continuous output currents.

B. Output Inductor L_o

The selection of inductor should in such a that the flow of current to be in continuous modes under normal operating conditions. The voltage at the dc bus converter will be excessive when the parameter of L_o can not be too high under light-load conditions.

C. Input Inductor L_{in}

In order to maintain the discontinuous operating mode for all conditions, the parameters for L_1 and L_2 should be sufficiently less, but it should not be very less in order to result in more peak currents. The input current is obtained by addition of currents flowing through the inductors i_{L1} and i_{L2}.

D. Flying Capacitor C_f

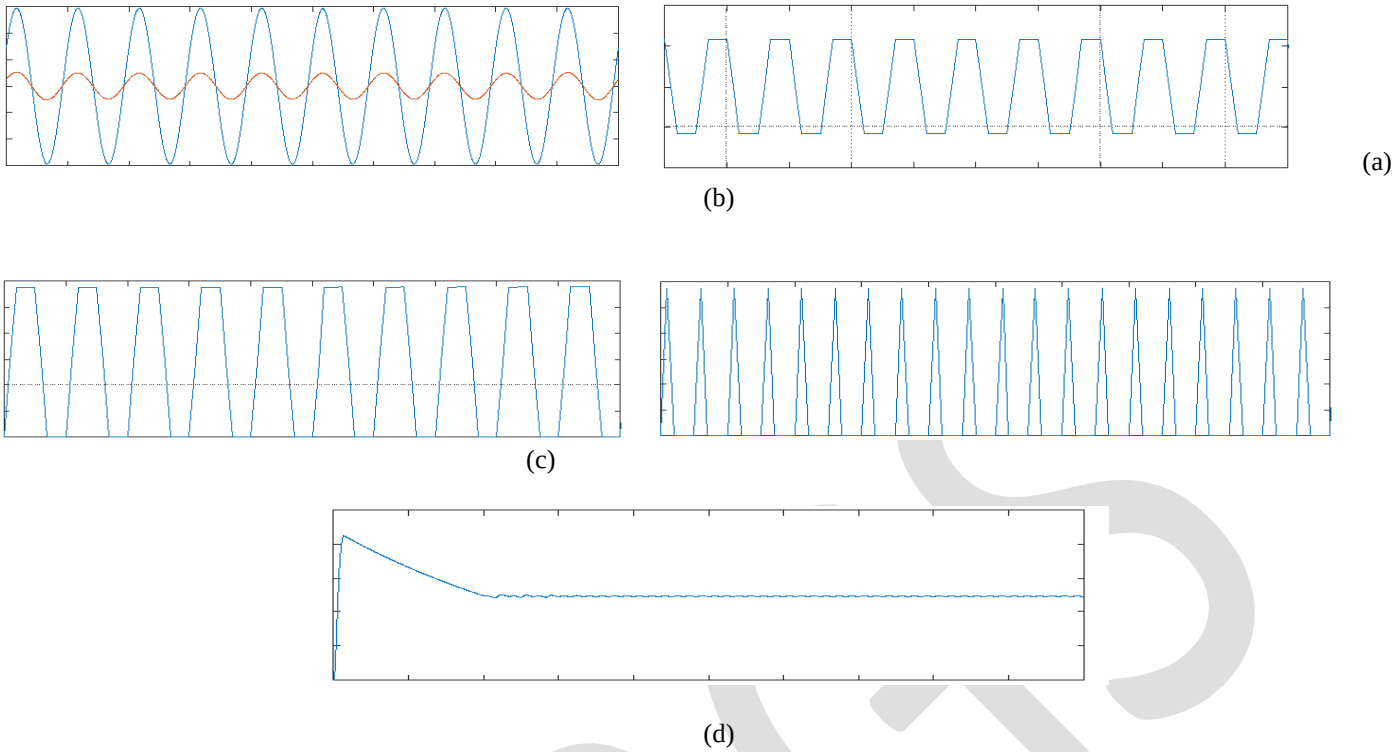
The flying capacitor is charged to half of the dc bus voltage. Whenever the converter is operated with phase-shift PWM control, flying capacitor is in general decoupled from the converter with the exception of at some stage in assured switching transitions, for instance switch S_1 stops conducting to start Mode 2 and whenever the switch S_4 starts conducting during the equivalent mode later in switching cycle; hence there is slight chance for C_f to charge and discharge through a switching cycle. Therefore, the converter can be intended according to the design procedure given in [21] as the operation of the two converters is identical.

5.SIMULATIONRESULTS

Table 1:

Input voltage V_{in}	208±10%v
Output voltage V_o	48v
Output power P_o	1.1 KW
Switching frequency f_{sw}	100kHz
Input inductor L_{in}	140uH
Output inductor L_o	100uH
Capacitors C_1 C_2 C_f	2200uF

The planned converter is implemented with phase-shift modulation using a UC 2879 phase-shift PWM IC. The main switches were IRFP27N60KPbF, and the diodes were UF1006DICT. The converters typical waveforms are shown in Fig. 4.



(a)

(b)

(c)

(d)

Fig.4. (a). Input voltage and current (b). Primary voltage of main transformer

(c).voltage and current at switchS_3. (d). output voltage

6.CONCLUSION

Interleaved three-phase three-level AC-DC single-stage PFC converter by using a standard phase-shift pulse width modulation was explained in this paper. . In this planned paper, the procedure of original converter is clarified and its features are discuss and its function is corresponding to another model converter. that the center tapped transformer is very costly to construct, which results same voltage lying on every half of the secondary windings. And the output is half of the secondary voltage, as each and every diode utilizes simply one half of the transformers secondary voltage. So that the output voltage of secondary winding of the transformer is double the times of the magnetizing voltage i.e; $2v_m$ when compared to the input power supply. Hence from the above discussion it is very clear that the cost of the circuit become expensive.

REFERENCES:

[1] Limits for Harmonic Current Emission (Equipment Input Current> 16A per Phase), IEC 1000-3-2, 1995.

[2] G. Spiazzi and F. C. Lee, “Implementation of single-phase boost power-factor correction circuits in three-phase applications,” IEEE Trans, Ind, Electron., vol. 44, no. 3, pp. 365-371, Jun. 1997.

[3] J. M. Kwon, W. Y. Choi, and B. H. Kwon, “Single-stage quasi-resonant flyback converter for a cost-effective PDP sustain power module,” IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2372-2377, Jun. 2011.

[4] H. L. Cheng, Y. C. Hsieh, and C. S. Lin, “A novel single-stage high-power-factor ac/dc converter featuring high circuit efficiency,” IEEE Trans. Ind. Electron., vol. 58, no. 2, pp. 524-532, Feb. 2011.

[5] H. S. Ribeiro and B. V. Borges, “New optimized full-bridge single-stage ac/dc converters,” IEEE Trans. Ind. Electron., vol. 58, no. 6, pp. 2397-2409, Jun. 2011.

[6] N. Golbon and G. Moschopoulos, "A low-power ac-dc single-stage converter with reduced dc bus voltage variation," IEEE Trans. Power Electron., vol. 27 , no. 8, pp. 3714-3724, Jan. 2012.

[7] H. M. Suraywanshi, M. R. Ramteke, K. L. Thakre, and V. B. Borghate, "Unity-power-factor operation of three phase ac-dc soft switched converter based on boost active clamp topology in modular approach," IEEE Trans. Power Electron., vol. 23, no. 1, pp. 229-236, Jan. 2008.

[8] U. Kamnarn and V. Chunkag, "Analysis and design of a modular three-phase ac-to-dc converter using CUK rectifier module with nearly unity power factor and fast dynamic response," IEEE Trans. Power Electron., vol. 24, no. 8, pp. 2000-2012, Aug. 2009.

[9] U. Kamnarn and V. Chunkag, "A power balance control technique for operating a three-phase ac to dc converter using single-phase CUK rectifier modules," in Proc. IEEE Conf. Ind. Electron. Appl., 2006, pp. 1-6.

[10] J. Contreas and I. Barbi, "A three-phase high power factor PWM ZVS power supply with a single power stage," in Proc. IEEE Power Electron. Spec. Conf. Rec., 1994, pp. 356-362.

[11] F. Cannales, P. Barbosa, C. Aguilar, and F. C. Lee, "A quasi-integrated AC/DC three-phase dual-bridge converter," in Proc. IEEE Power Electron. Spec. Conf. Rec., 2001, pp. 1893-1898.

[12] F. S. Hamdad and A. K. S. Bhat, "A novel soft-switching high-frequency transformer isolated three-phase AC to DC converter with low harmonic distortion" IEEE Trans. Power Electron., vol. 19, no. 1, pp. 35-45, Jan. 2004.

[13] P. M. Barbosa, J. M. Burdio, and F. C. Lee, "A three-level converter and its application to power factor correction," IEEE Trans. Power Electron., vol. 20, no. 6, pp. 1319-1327, Nov. 2005.

[14] C. M. Wang, "A novel single-stage high-power-factor electronic ballast with symmetrical half-bridge topology," IEEE Trans. Ind. Electron., vol. 55, no. 2, pp. 969-972, Feb. 2008.

[15] P. M. Barbosa, J. M. Burdio, and F. C. Lee, "A three-level converter and its application to power factor correction," IEEE Trans. Power Electron., vol. 20, no. 6, pp. 1319-1327, Nov. 2005.

[16] Y. Xie, Y. Fang, and H. Li, "Zero voltage-switching three-level three-phase high-power-factor rectifier," in Proc. IEEE Ind. Electron. Soc. Conf. Rec., 2007, pp. 1962-1967.

[17] B. Tamyurek and D. A. Torrey, "A three-phase unity power factor single stage ac-dc converter based on interleaved flyback topology," IEEE Trans.Power Electron., vol. 26, no. 1, pp. 308-318, Jan. 2011.

[18] M. Narimani and G. Moschopoulos "A novel single-stage multilevel type full-bridge converter," IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 31-42, Jan. 2013.

[19] A. M. Cross and A. J. Forsyth, "A high-power-factor, three-phase isolated ac-dc converter using high-frequency current injection," IEEE Trans. Power Electron., vol. 18, no. 4, pp. 1012-1019, Jul. 2003.

[20] M. Narimani and G. Moschopoulos "A new interleaved three-phase single-stage PFC AC-DC converter," IEEE Trans. Ind. Electron., vol. 60, no. 1, pp. 648-654, Feb. 2014.

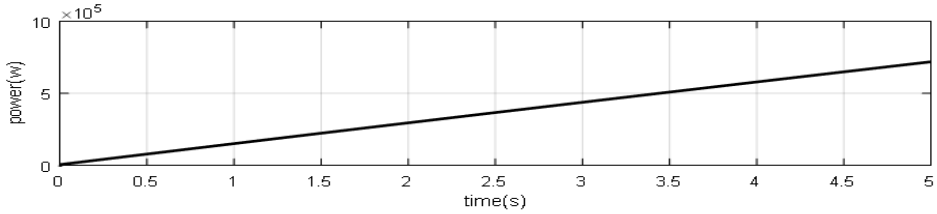
[21] M. Narimani and G. Moschopoulos "A new interleaved three-phase single-stage PFC AC-DC converter," IEEE Trans. Ind. Electron., vol. 30, no. 7, July. 2015.

[22] B. Tamyurek and D. A. Torrey, "A three-phase unity power factor single-stage ac-dc converter based on an interleaved flyback topology," IEEE Trans. Power Electron., vol. 26, no.1, pp. 308-318, Jan. 2011.

[23] N. Rocha, C. B. Jacobina, and C. D. Santos, "parallel connection of two single-phase ac-dc-ac three-leg converter with interleaved technique," in Proc. IEEE Ind. Electron. Soc. Conf., 2012, pp. 639-644.

Load 1 and load 2 are operating from t=0.5 to 1.5 and 1 to 1.5 at 3kw power. At this time interval power from comes from the grid to load. So grid power is negative at this time it means load was feed by the grid. After t=2 sec grid was continuously in off state. From this time battery power was come into picture which was shown in Fig5.2 (b). From t=2sec to t=2.5sec solar generated power was stored in battery. Now at 2kw power, at the time t=2.5sec load 1 was started and operates continuously till t=3.5 sec .t=3sec to t=3.5sec load 2 was operating with the power of 2kw. At this time interval these 2 loads feed by the battery power.

Results



(a)

Fig 5.1 a. Dc power

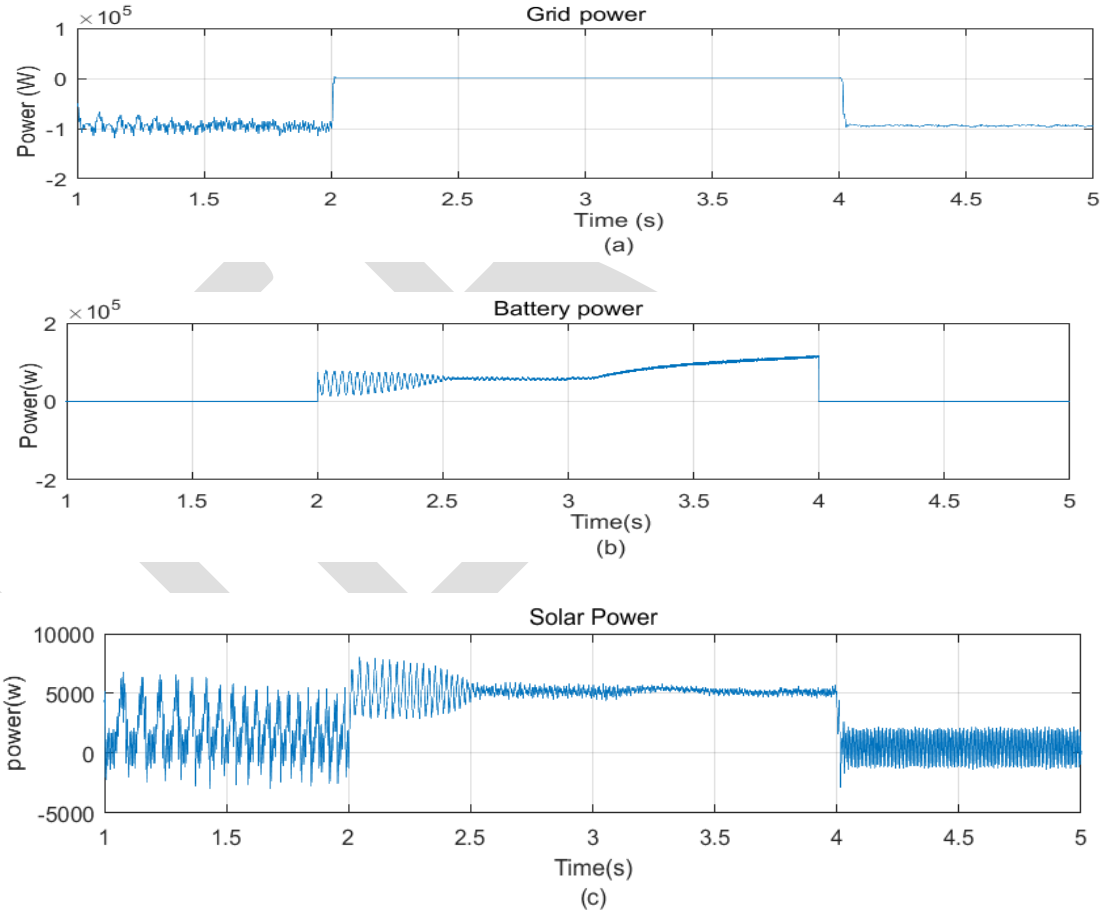


Fig 5.2: a. grid power, b. battery power, c. solar power.