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A Comparative review and analysis of different phase frequency detectors for Phase Locked Loops

Anu Tonk

Department of Electronics & Communication Engineering,

F/o Engineering and Technology,

Jamia Millia Islamia, New Delhi

tonkanu.saroha@gmail.com

Abstract---This paper presents phase frequency detectors (PFDs) with the five different designs which are Standard gate based logic, DCVSL, TSPC logic, CML logic and Modified CML logic The simulation results are focused on accounting the frequency operation of PFDs considering an input frequency of 100 MHZ .The PFDs have been designed using 0.35μm CMOS technology on SPICE simulator with 3.3V supply voltage. All PFDs are designed to be dead zone free. Results reported in the paper compare and concentrate on fast frequency operation, a low output noise, dead zone and power dissipation. When compared to all the logics S_PFD consumes least power, the minimum delay is experienced by TSPC_PFD and Modified CML_PFD. DCVSL_PFD observes the least output noise.

Keywords--- Phase frequency detectors, Phase locked loops, CML_PFD, Modified Current Mode Logic M_CML_PFD, True Single-Phase Clock PFD (TSPC_PFD), Differential Cascode Voltage Switch Logic PFD (DCVSL_PFD)

INTRODUCTION

A PLL comprises of several components [1] which are (1) phase or frequency detector, (2) charge pump, (3) loop filter, (4) voltage-controlled oscillator, and (5) frequency divider. Phase Locked Loops (PLL) has a negative feedback control system circuit. Our study is focused on designing phase frequency detectors (PFD) using different CMOS design techniques with the aim to compare the different logic based PFDs in terms of power consumption ,delay and speed of the block . The design has been validated using S-Edit at 350 nm technology with Tanner as simulator. There can be various methods of phase and frequency detection. XOR gate based detection but it is less preferred compared to the PFD where two signals are generated named [2] UP and DOWN with its pulse width proportional to the phase difference .This difference indicates the PLL that whether the feedback signal lags or leads the reference signal respectively. The reason behind rejecting use of XOR gate as detector was that that it can lock onto harmonics of the reference signal and most importantly it cannot detect a difference in frequency. These disadvantages were overcome by another type of PFD which only responds to edges of the two inputs and are free from false locking to harmonics unlike XOR based detector. The methodology of low-jitter PLL design has been developed in recent years. The jitter of PLL primarily is contributed from the reference clock, phase frequency detector, supply noise, substrate noise, charge pump circuit and VCO internal noise. However, power-supply noise generated by large switching digital circuits perturbs the analog circuits used in the PLL. The output clock period may change with the power-supply noise and with other sources of noise (for example, thermal noise in MOS devices). It is common to refer to this change as jitter, which is the variation of the clock period from one cycle to another cycle compared to the average clock period.[5] The clock jitter directly affects the maximum running frequency of the circuit because it reduces the usable cycle time. When the clock period is small, the digital circuits in the critical path may not have enough usable time to process the data in one period, resulting in the failure of the circuit. We have safely selected our design specifications for 350 nm technology for having less higher order effects and as well as achieving higher S/N ratio, which degrades as lower we go with the technology because our main aim was to study the behavior of the Phase frequency detectors without much higher order effects in prominence. Conventional PFD suffers from a major problem called dead zone. The dead-zone problem occurs when the rising edges of the two clocks to be compared are very close. Due to lots of reasons such as circuit mismatch and delay mismatch, the PFD has a difficulty in detecting such a small difference. The PFD doesn't detect the phase error when it is within dead zone region, then PLL locks to a wrong phase. A conventional CMOS PFD has no limit to the error detection range. Therefore, the capture range of PLL is only limited by the Voltage Controlled Oscillator (VCO) output frequency range [9]. The capture range of PLL is determined by the error detection range of PFD. Different designs have been used here for the purpose of observation and comparison with the outputs obtained using other logic designs.

1. DIFFERENT LOGIC BASED DESIGNS OF PFD

Standard CMOS (S_PFD), True Single-Phase Clock PFD (TSPC_PFD), DCVSL Differential Cascode Voltage Switch Logic PFD (DCVSL_PFD), Current Mode Logic PFD (CML_PFD) and Modified Current Mode Logic PFD (M_CML_PFD) circuits have been considered here. The high speed operation of MOS transistors is limited by their low transconductance. Therefore, dynamic and sequential circuit techniques or clocked logic gates such as, true single phase clock must be used in designing synchronous circuits to reduce circuit complexity, increase operating speed, and reduce power dissipation. [3]The key benefits of DCVSL are its low input capacitance, differential nature and low power consumption.

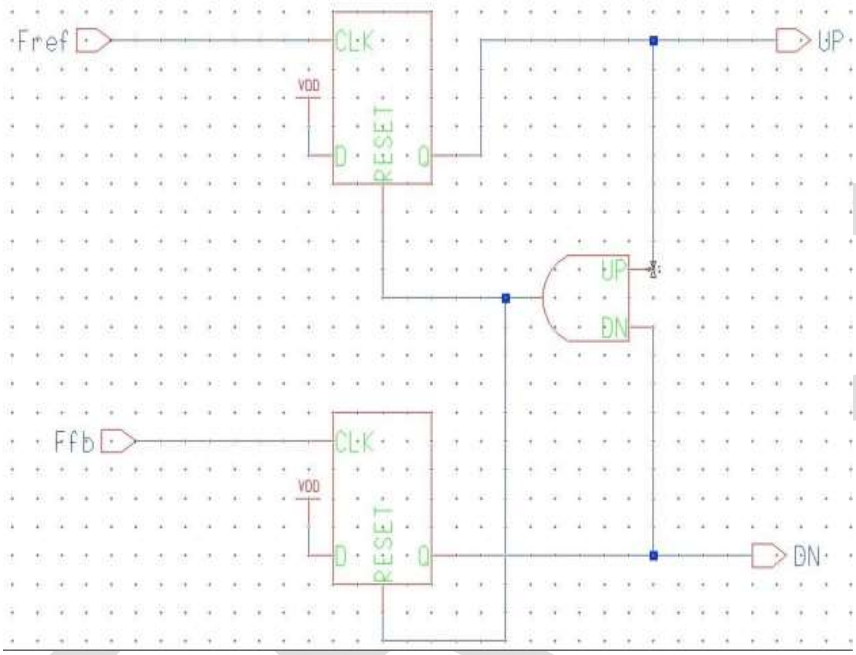

Fig.1. Phase Frequency Detector circuit (PFD)

1.1 Standard CMOS phase frequency detector (S_PFD): Conventional pull-up PMOS, pull-down NMOS static logic is popular because of its convenient availability in standard library cells, small area usage, low power dissipation, and high noise margins[7]. Even though the static power consumption of the conventional CMOS logic gate is zero ideally, it dynamically generates a large current pulse flowing from the power supply to the ground during the state transition. The coupling of the high switching spike noise may cause crosstalk between the analog and the digital circuitry. Even worse, the switching noise might induce latch up which can possibly destroy devices with the integrated circuit due to overheating [11], [12]. Standard CMOS PFD is designed using the conventional approach. There are two outputs from the PFD named UP and DOWN.

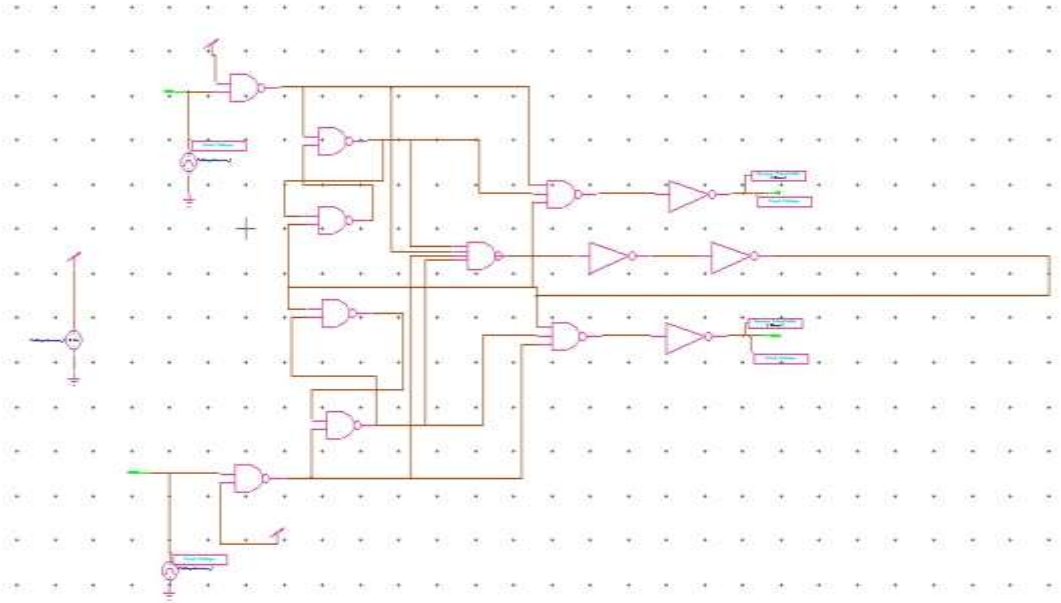

Fig2. Standard CMOS (S_PFD) Phase Frequency Detector circuit

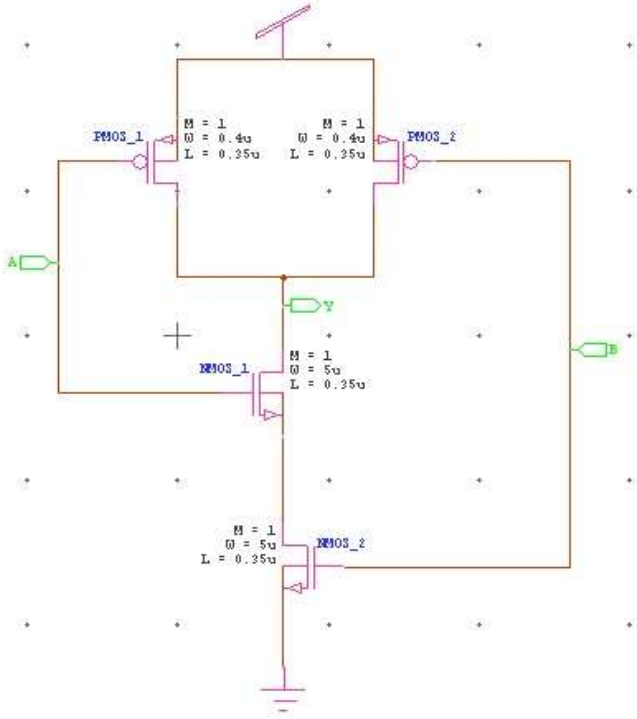

Fig.3. NAND cell for Standard CMOS (S_PFD) Phase Frequency Detector

In Fig 4 we can see that the reference signal and feedback signal frequency are different and accordingly we get the UP and DOWN signals depicting which of the two signals was leading or lagging and by how much phase. The Fig 5 shows the PFD characteristics when output of VCO or feedback signal (fback) and reference frequency (fref) are of same frequencies. In this we can observe that whenever both the falling edges of fback and fref occur simultaneously, there will be a glitch on up and down signal showing that the two frequencies are locked in phase as well as frequency.

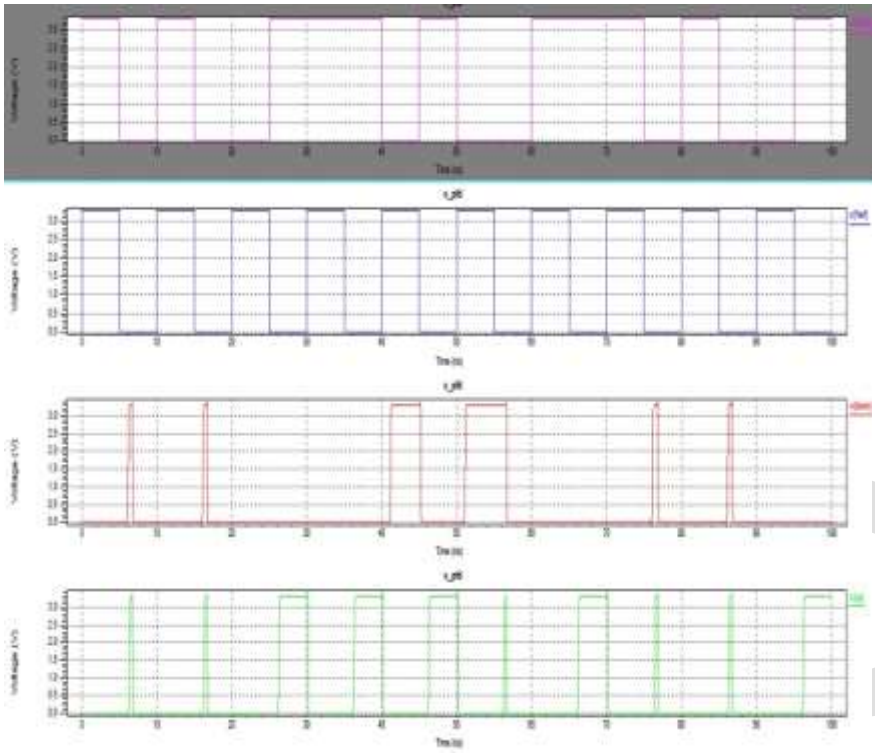

Fig.4. PFD output when both feedback and reference frequency are different. (Lead/lag at different instants).

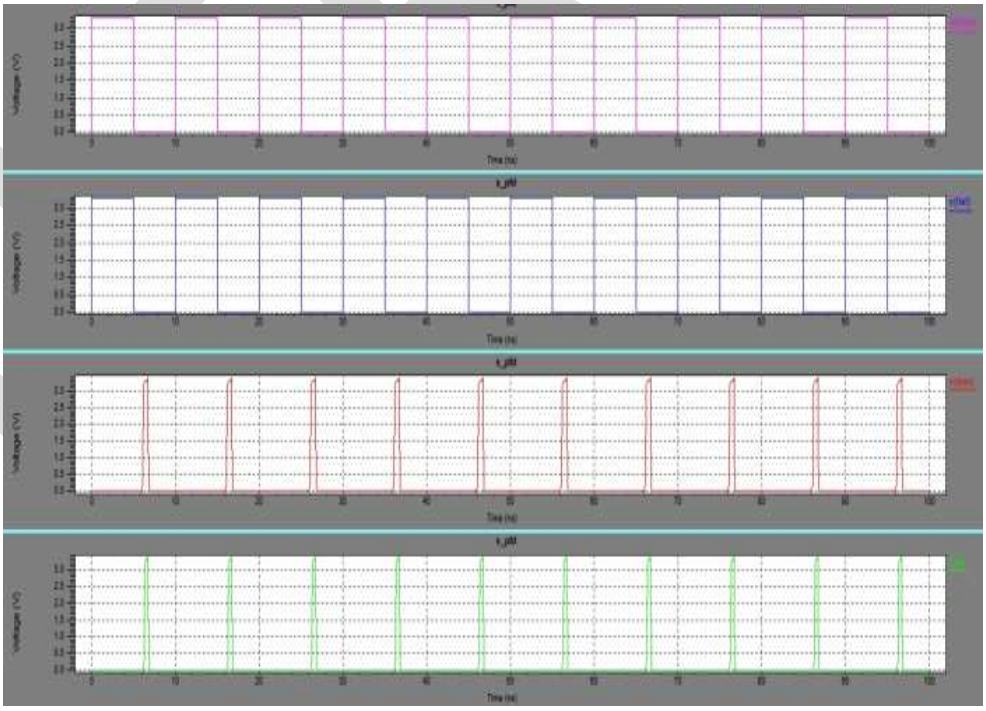

Fig.5. Output of S_PFD depicting PLL in locked state when both feedback and reference frequencies are same.

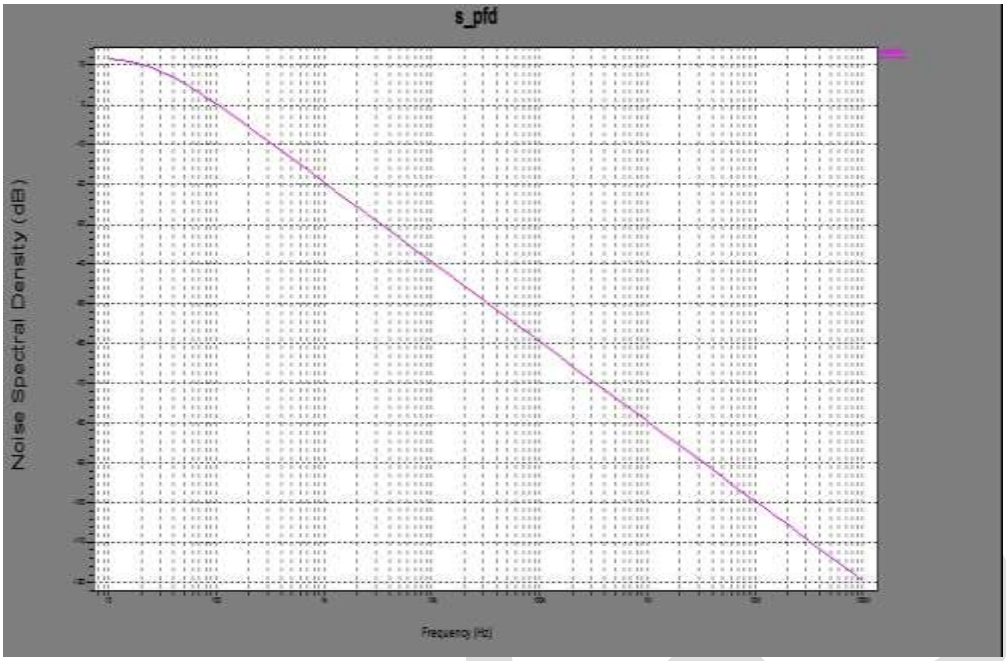

Fig.6. Noise Spectral Density graph for S_PFD (on x axis frequency range is from 10 to 100 MHz, on y axis noise in db)

1.2 Differential cascode voltage switch logic pfd (DCVSL_PFD): DCVSL has several advantages over the conditional CMOS static logic. It does not require a complementary pull up network, thus the parasitic capacitances at the output are reduced, which produces a faster response. Secondly, in contrast to pseudo-NMOS, its output voltages can swing from rail to rail and there is no direct path between VDD and ground in steady states. Finally it generates both true and complementary outputs and an inverting stage can be eliminated and its performance is further improved. [4]DCVS logic is responsible for the realization of faster circuits than are possible with conventional forms of CMOS logic, but this speed advantage is often achieved at the expense of circuit area and active power consumption.

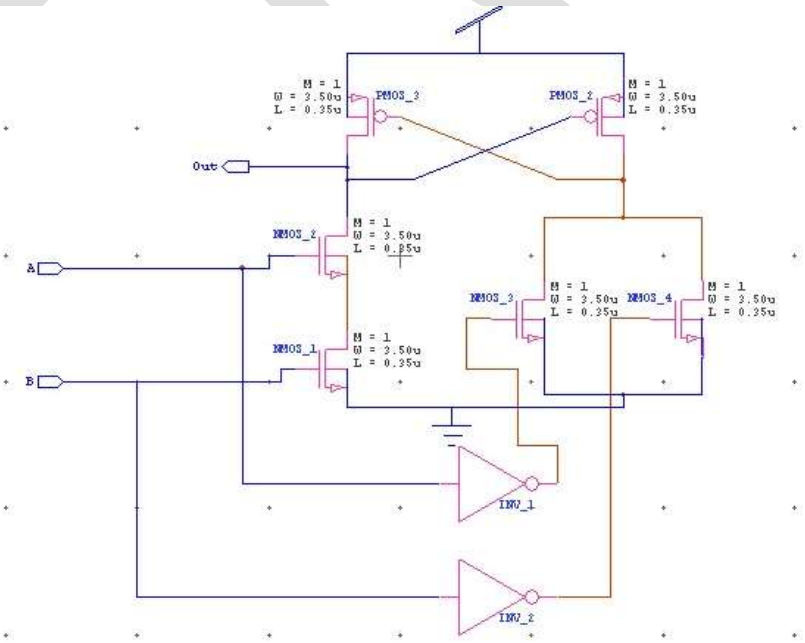

Fig.7. NAND cell for DCVSL [6] Phase Frequency Detector

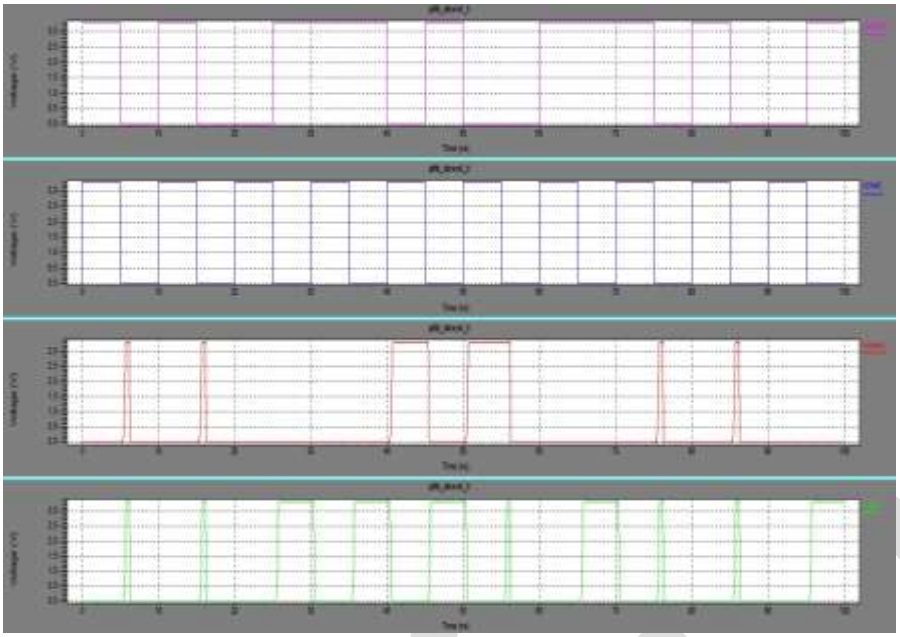

Fig.8. Output of DCVSL_PFD depicting PLL state when both feedback and reference frequencies are different, (lead/lag at different instants).

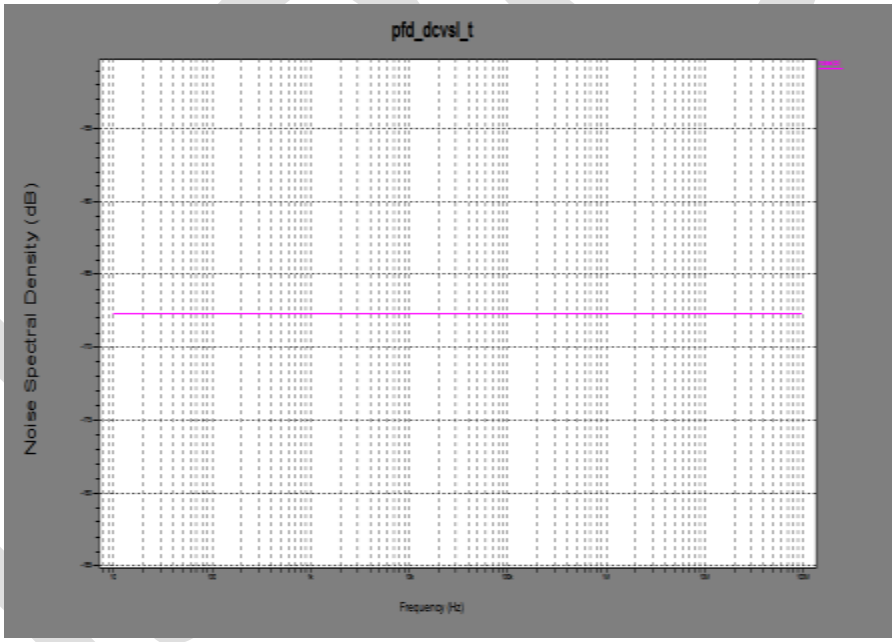

Fig.9.Noise Spectral Density graph for DCVSL_PFD (x axis represents a frequency range from 10 to 100 MHz and y axis represents noise in db)

1.3 True single phase clock pfd(TSPC_PFD): We have designed it as a negative edge triggered pfd. Here two signals are given, one is v_{ref} and other is v_{back}. If either of two signal have negative edge first that one will be leading. Suppose v_{back} fall down before v_{ref} then v_{down} signal at output will become high it means v_{back} is leading as can be seen in Fig 11.

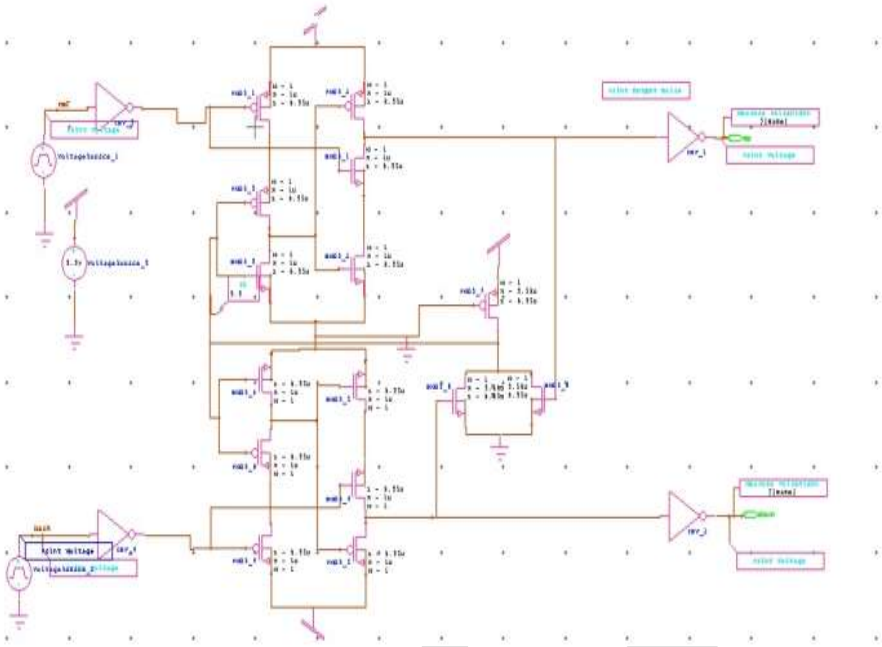

Fig. 10.Schematic for TSPC[8] Phase Frequency Detector

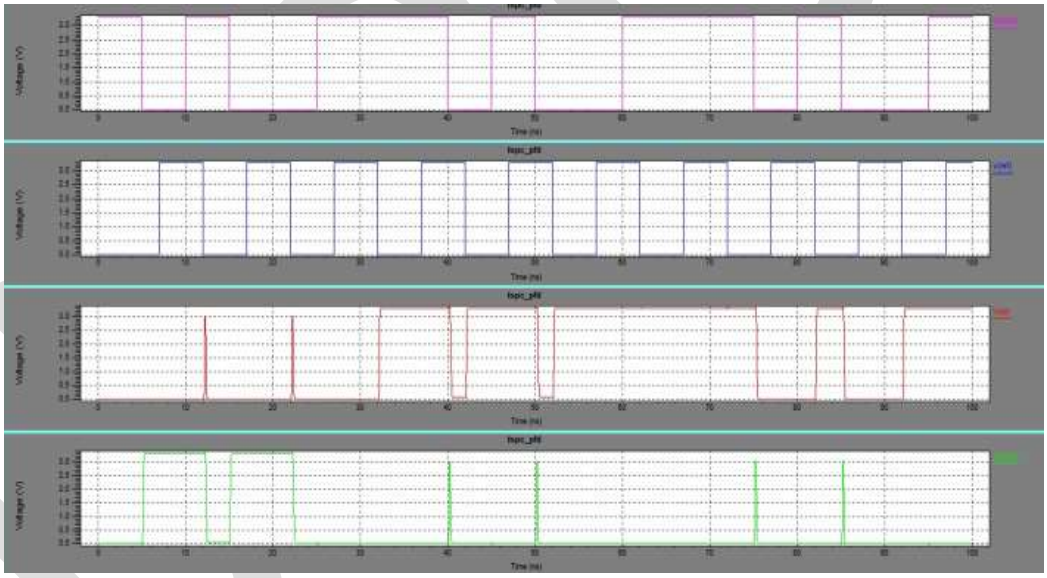

Fig.11. Output of TSPC_ PFD depicting PLL state when both feedback and reference frequencies are different, (lead/lag at different instants).

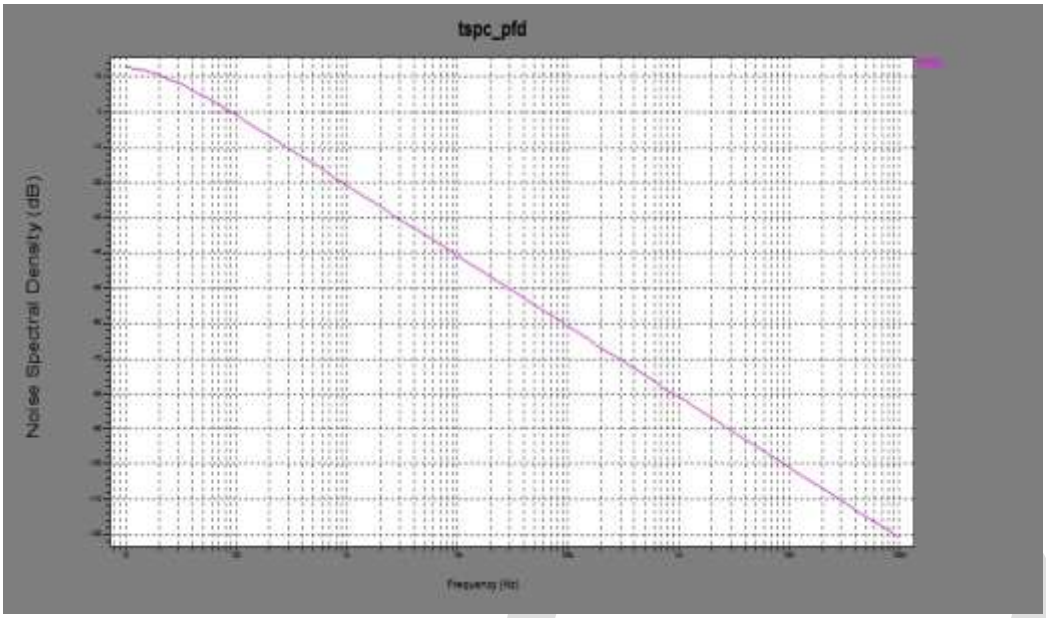

Fig.12. Noise Spectral Density graph for DCVSL_PFD (x axis represents a frequency range from 10 to 100 MHz and y axis represents noise in db)

1.4 Current mode logic (CML_PFD)[8]*:* In CML PFD, two d-latch are connected in such a way that they can work as PFD as depicted in Fig 14. The block diagram of two stages D flip flop is shown in Figure14 .A current mode logic (CML) structure is used to reduce the switching noise and power supply noise [10]. The CMOS logic has the advantage of low power consumption at low frequency operation. The CML requires two lines for each signal. Therefore, the area of CML is two to four times larger than in the CMOS logic. In high frequency operation the CML logic is consumption power less than CMOS logic.

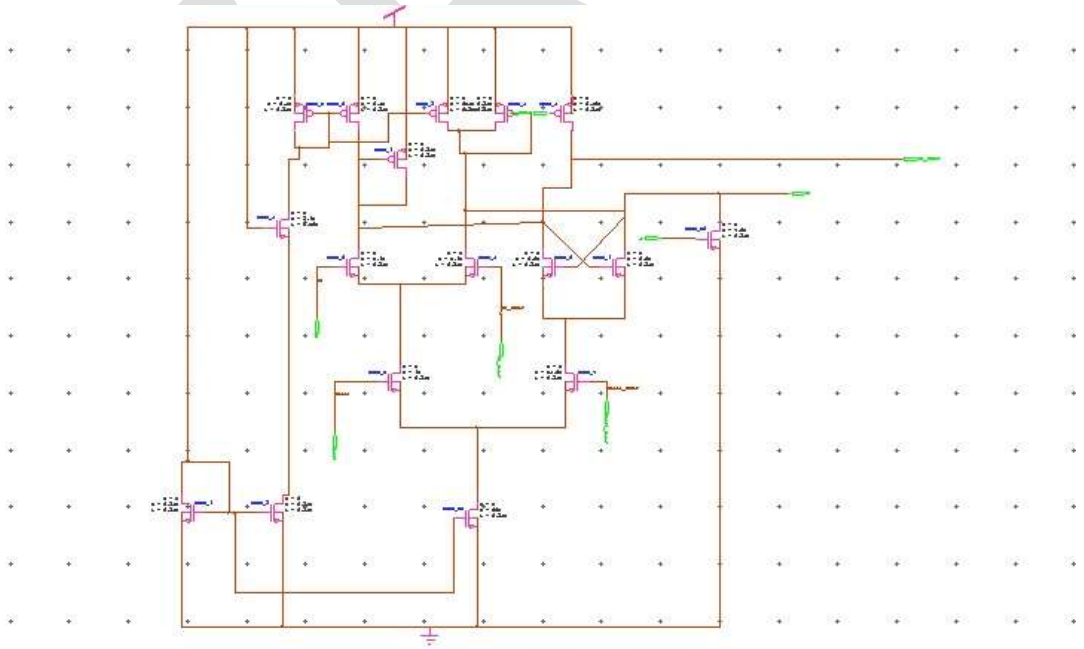

Fig.13. Schematic of D latch for CML [8] Phase Frequency Detector

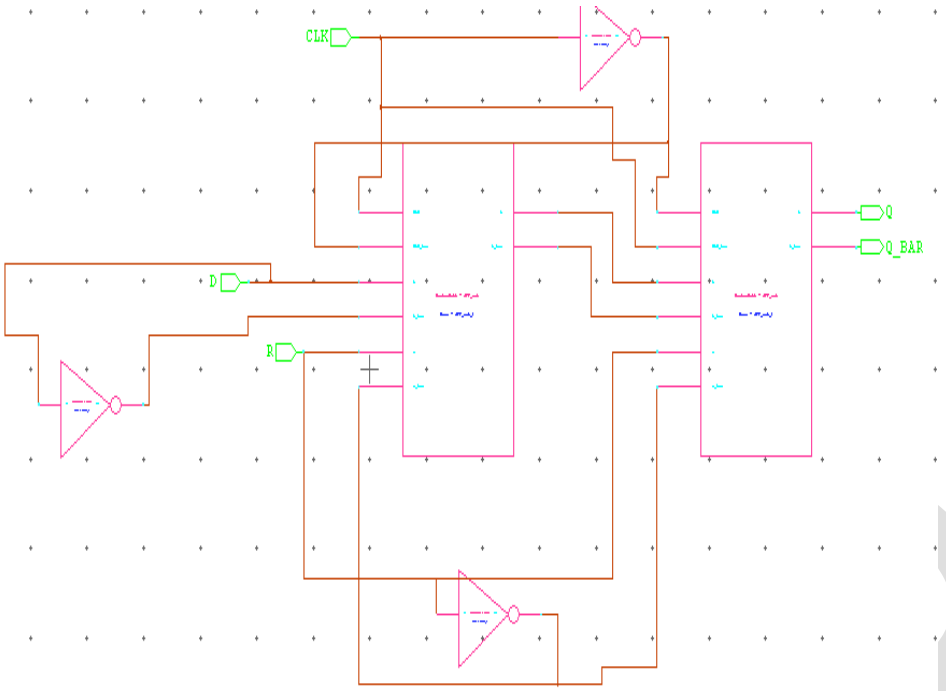

Fig.14. Schematic of D latch to D Flip flop conversion for CML [8] Phase Frequency Detector

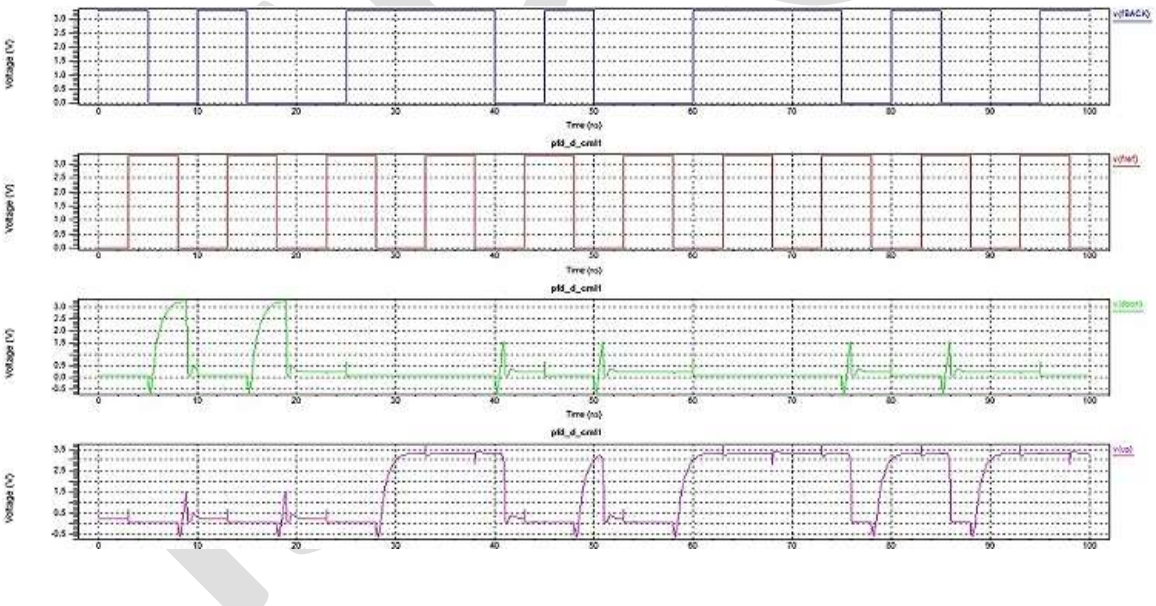

Fig.15. Output of CML_ PFD depicting PLL state when both feedback and reference frequencies are different, (lead/lag at different instants).

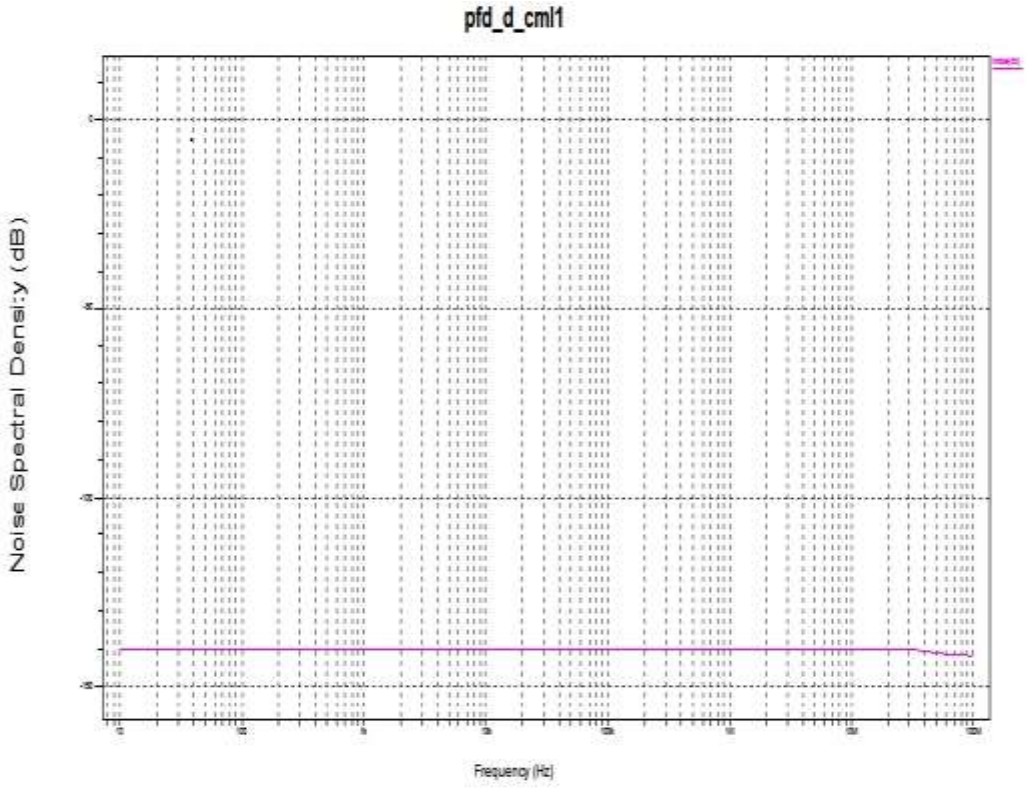

Fig.16. Noise Spectral Density graph for CML_PFD (x axis represents a frequency range from 10 to 100 MHz and y axis represents noise in db)

1.5 Modified CML pfd (M_CML_PFD): In the Modified CML, the number of transistors in M_CML_PFD d latch is reduced with the removal of two transistors pmos_2 and pmos_3 which form current mirrors. Thus, Power consumption and delay of the current mode logic based M_CML_ PFD is observed to be reduced.

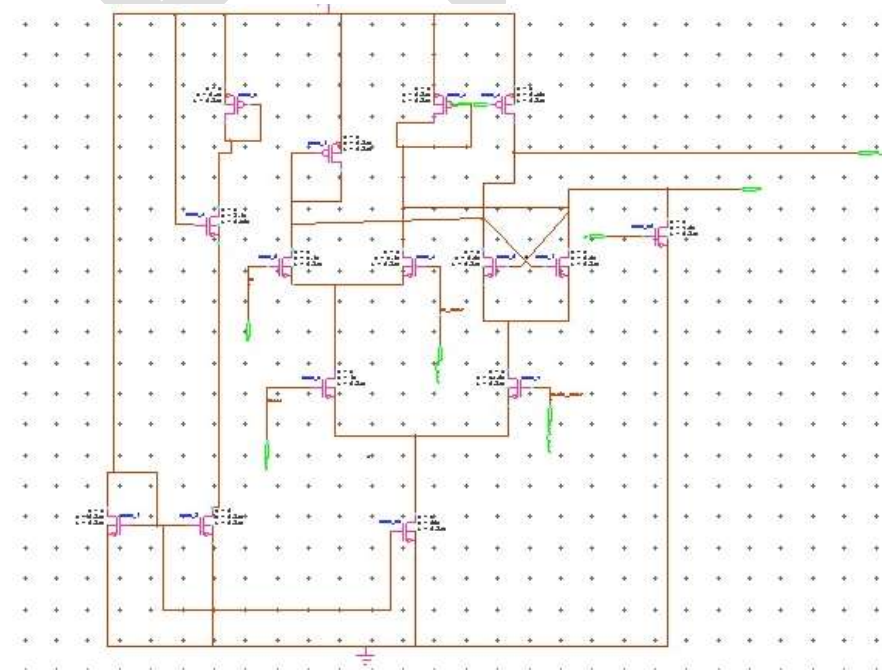

Fig.17. Schematic of D latch for M_CML Phase Frequency Detector

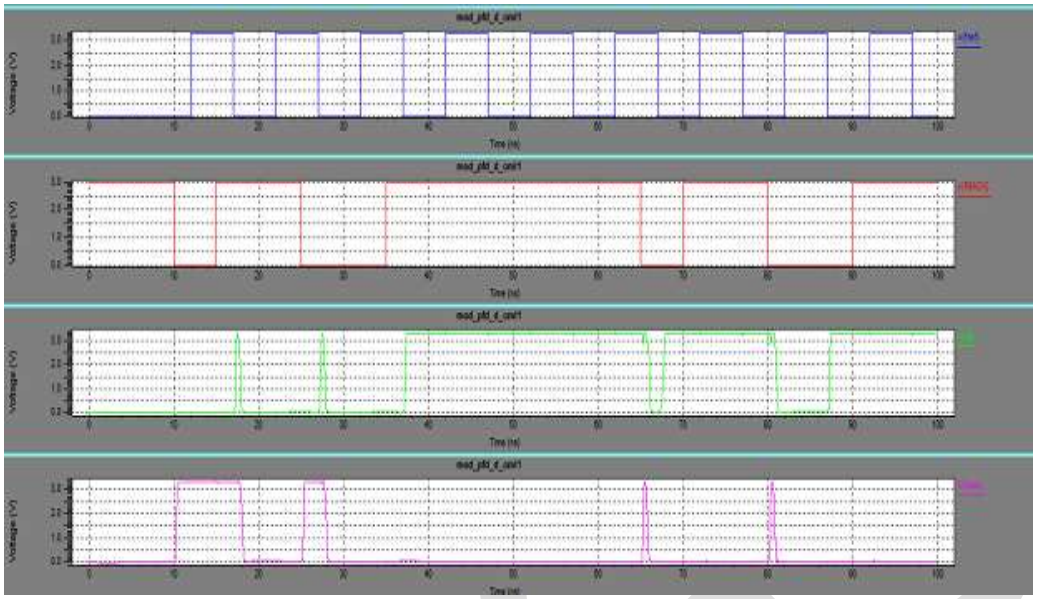

Fig.18. Output of M_CML_ PFD depicting PLL state when both feedback and reference frequencies are different, (lead/lag at different instants).

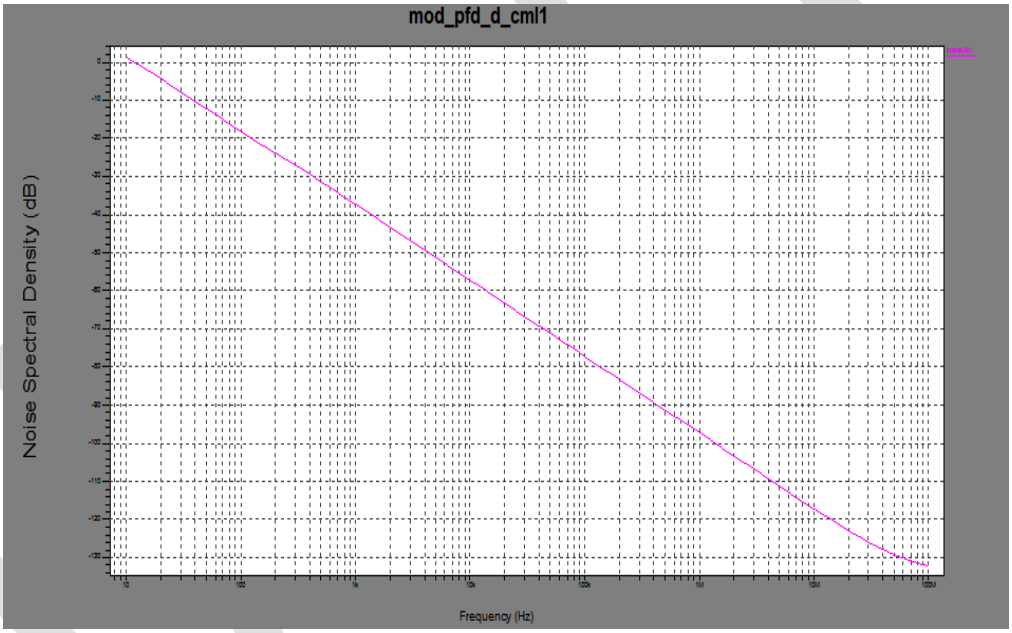

Fig.19. Noise Spectral Density graph for M_CML_PFD (x axis represents a frequency range from 10 to 100 MHz and y axis represents noise in db)

1.6 Simulations

The simulations mentioned above were done using Tanner tools 14 version. With the help of S-EDIT, W-EDIT, L-EDIT net list was generated and SPICE commands were used to obtain various parameters mentioned in the Table 1.

Table 1: Setup Parameters:

Rise time/RT	0.01 ns
Fall time/FT	0.01ns

High Time/HT	5ns
Low time/LT	5ns
Pulse Width/PW	5ns
Bit pattern	1010011
AC analysis(Frequency Sweep Type)	dec
Start frequency ; Stop frequency	10 meg; 100 meg
Number of frequencies	10

RESULTS

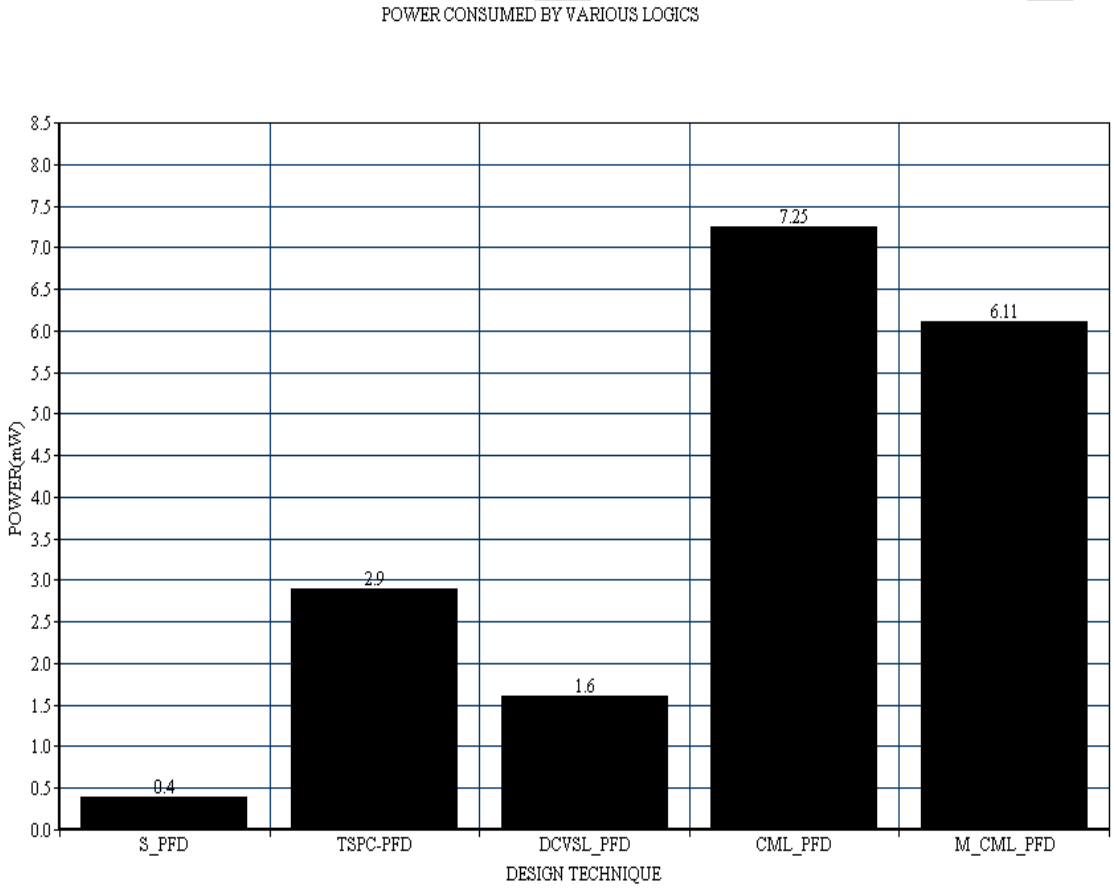

Fig.20. Power consumed by various PFDs

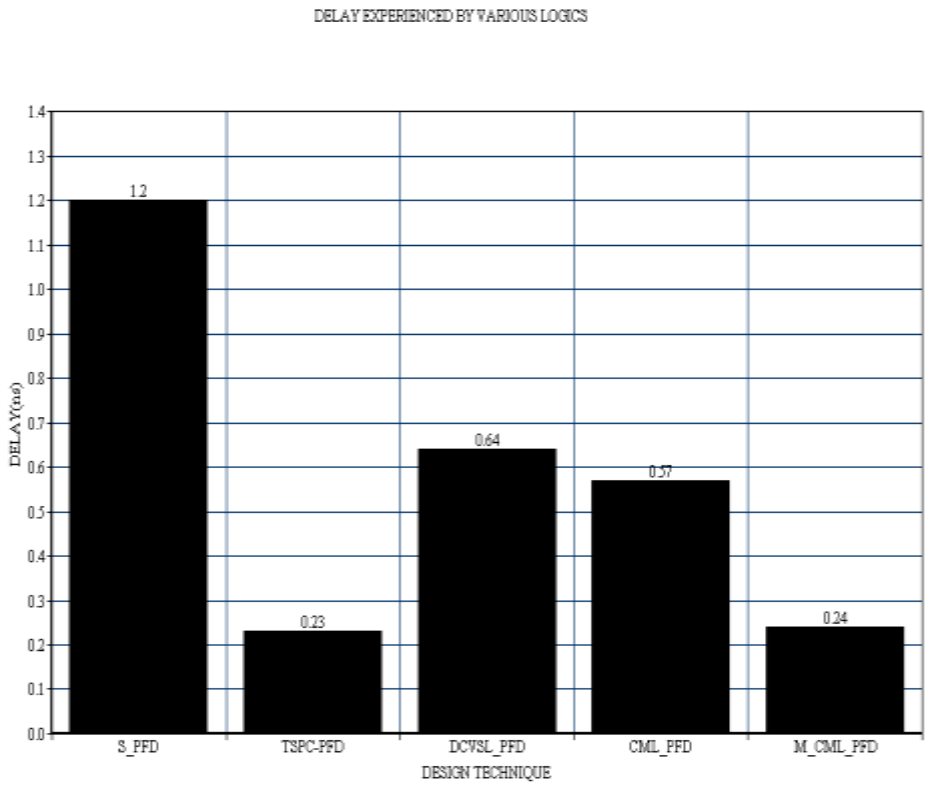

Fig.21. Delay experienced by various PFDs

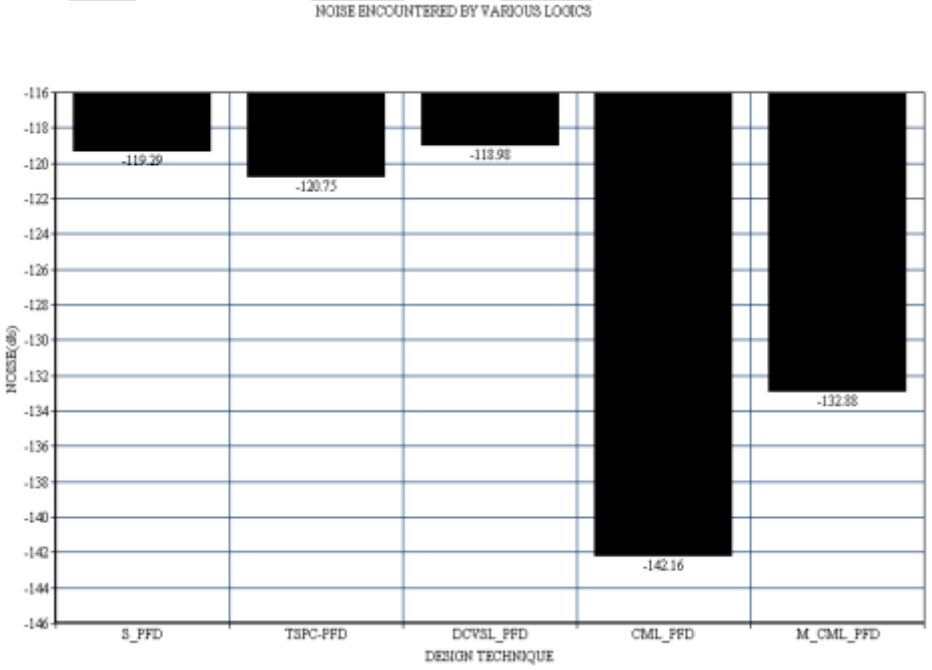

Fig.22. Noise encountered by various PFDs

Table 2: Comparison of different schemes of PFD:

	S_PFD	TSPC_PFD	DCVSL_PFD	CML_PFD	M_CML_PFD
Power	0.4mW	2.9mW	1.6mW	7.25mW	6.11mW
Glitch time	0.6ns	0.16ns	0.38ns	0.08	0.56ns
Glitch period	10ns	10ns	10ns	10ns	10ns
Delay	1.2ns	0.23ns	0.64ns	0.57ns	0.24ns
Output noise	-119.29db	-120.75db	-118.98db	-142.16db	-132.88db

CONCLUSIONS

We successfully compared and implemented five designs of PFD which are as follows:

- NAND gate based standard phase frequency detector, DCVSL_PFD, TSPC_PFD, CML based PFD and M_CML_PFD.
- It was found that the designed PFD using standard Nand gates consume 0.4mW power, PFD using DCVSL logic consume 1.6mW and the TSPC PFD consumes 2.9mW with the power supply of 3.3V.
- The TPSC_PFD_PFD and M_CML_PFD experience minimum delay among all the PFD designs and can be used for faster speed of operation.
- All the models are designed to be dead zone free.
- The locking time of 10ns is obtained for the different designs with reference and input frequencies equal and of value 100MHZ.
- The S_PFD design and DCVSL_PFD design can be used for low output noise with DCVSL output noise being least and equal to -118.98db. Thus, S_PFD and DCVSL_PFD are best suitable for low power operations which also observe low output noise.

Table 2 depicts the difference in values for various parameters of all the five designs.

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